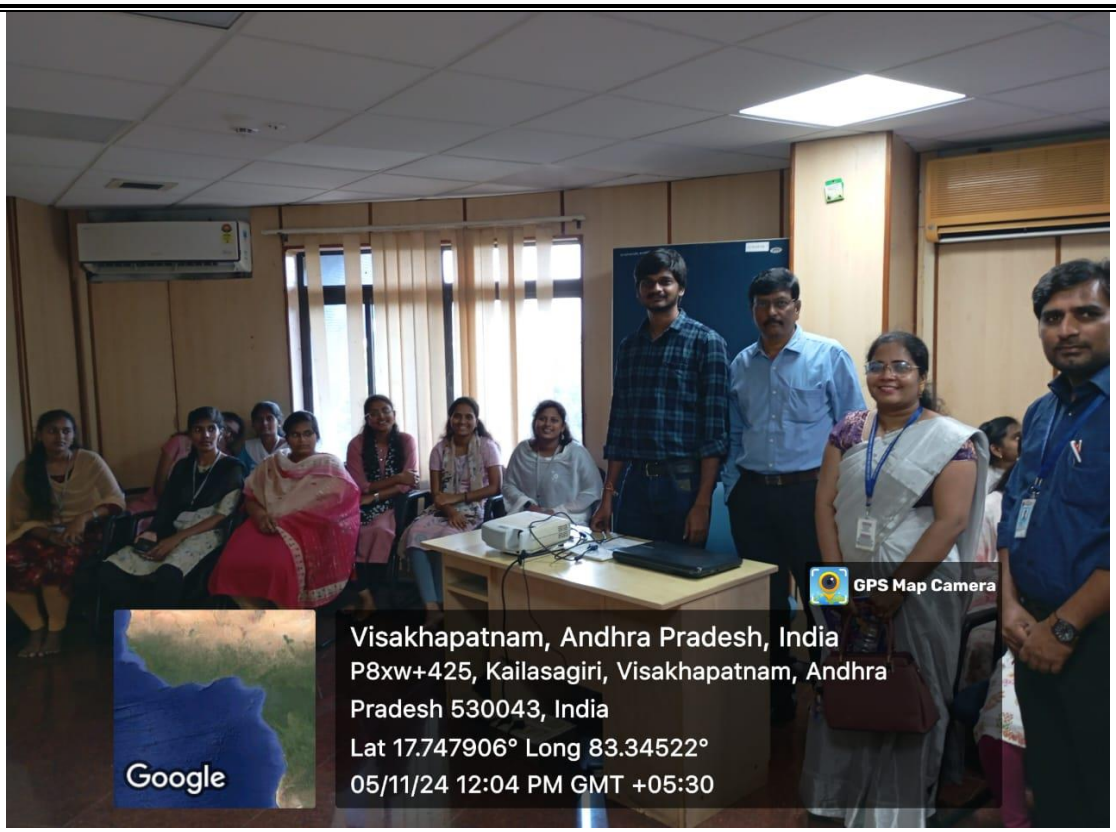
Report on one day industrial visit to Doppler Weather Radar Station, Kailasagiri on 5.11.2024

The Department of Electronics and Communication Engineering, in collaboration with the IETE Students' Forum, organized a one-day industrial visit to the Doppler Weather Radar Station in Kailasagiri on 05.11.2024 for the IV/IV B.Tech ECE students.

Students at the entrance of DWR, Kailasagiri

The primary goal of the visit was to familiarize students with the various equipment used in the medical field and their applications within the company. The students were divided into two batches for the visit, allowing them to explore and gain hands-on experience. The exposure to Doppler Weather Radar provided valuable insights into its practical applications.



Students and faculty members with DWR staff

The students expressed their gratitude to the department for organizing this insightful industrial visit, which helped them align their skills with industry needs. The department also extends its thanks to the authorities of the Indian Meteorological Department's Doppler Weather Radar Station in Visakhapatnam for granting permission and providing guidance throughout the visit.

HOD, ECE

REPORT

“OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE”

Date: 16th December 2024 – 21st December 2024,

Institute Name: GAYATRI VIDYA PARISHAD COLLEGE FOR DEGREE AND PG COURSES (A),

ENGINEERING AND TECHNOLOGY PROGRAM

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

ATAL FDP on "OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE"

The Department of Electronics and Communication Engineering organized a Six-day Faculty Development Program (FDP) on "OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE" under ATAL Sponsored FDP, 185 participants all over the country registered for this FDP, out of which 130 participants participated in all the FDP sessions. The feedback from the participants is very good and the content delivered by all the resource persons is informative.

The speakers for the 6-day FDP on "OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE" were:

Mr. Dilip Yenni, Technical Manager Quest Global, Hyderabad

Mr. Dilip Yenni: He is highly experienced VLSI Backend Physical Design professional with 10+ years of industry expertise in designing and delivering high-quality semiconductor solutions. Skilled in leading technical teams, managing complex projects, and driving innovation in physical design methodologies. Proven track record in technical leadership roles with a deep understanding of ASIC design, floor planning, place-and-route (PnR), clock tree synthesis (CTS), and signoff processes. Currently serving as a **Technical Manager** at Quest Global, Hyderabad, leveraging a hands-on approach to manage cross-functional teams, optimize project outcomes, and deliver cutting-edge designs. Prior to this, demonstrated outstanding leadership as a **Technical Lead** at AdeptChip Services Pvt. Ltd., Bangalore, for 8 years, where he contributed to the successful delivery of multiple high-performance chip designs for global clients.

Mr.Sujan, CEO & Cofounder , Enium , Bangalore

Mr. Sujan is the CEO and Co-Founder of **Enium**, a leading technology company based in Bangalore. He holds a **Bachelor of Technology (B.Tech)** degree in **Electronics and Communication Engineering (ECE)** from **JNTU Kakinada**. With **9 years of extensive experience** in **VLSI Back-End Physical Design**, Mr. Sujan has made significant contributions to the semiconductor industry.

Before establishing Enium, he worked as a **Technical Lead** at **Lead SO Bangalore**, where he honed his expertise in VLSI design and implementation. His leadership and technical acumen have been instrumental in driving innovation and excellence in the field.

Ms. Rashmi, Senior Lead Engineer , Lead SOC Bangalore

Ms. Rashmi is a skilled VLSI Backend Physical Design engineer with **7 years of industrial experience**, specializing in delivering high-quality semiconductor solutions. Currently serving as a **Senior Lead Engineer** at **Lead SOC**, she has been contributing to cutting-edge SOC design projects since 2020.

With a strong foundation in Electronics and Communication Engineering, earned during her **B.Tech at Jawaharlal Nehru Technological University (JNTU)** from 2013 to 2016, Rashmi combines technical expertise with problem-solving abilities to meet and exceed design specifications. Her work is characterized by precision, efficiency, and adherence to the highest industry standards.

Mr Udaya Kumar E, Senior Lead Engineer, Lead SOC Hyderabad

Mr. Udaya Kumar E , Senior Lead Engineer has In-depth hands-on experience in block-level design implementation from floor planning to routing, ensuring optimized and high-quality designs. Expertise in industry-standard tools for floor planning, placement, routing, and timing analysis. and Proficient with sign-off tools for Static Timing Analysis (STA) and Timing-ECO generation. He completed M.E. (Communication Systems) from Sri Ramakrishna Institute of Technology and B.E. (Electronics and Communication Engineering) from Kalaignar Karunanidhi Institute of Technology.

Mr. Hari. Lead Engineer, Quest Global, Visakhapatnam.

Mr. Hari T is a dedicated and detail-oriented **VLSI Backend Physical Design Engineer** with **4 years of experience**, currently serving as a **Lead Engineer** at **Quest Global**, Vizag. His expertise lies in delivering efficient and high-quality VLSI backend solutions, specializing in floorplanning, placement, routing, and timing closure for complex semiconductor designs.

With a solid educational background, Mr. Hari holds an **M.Tech in VLSI** and a **B.Tech in Electronics and Communication Engineering (ECE)** from **Jawaharlal Nehru Technological University (JNTU)**. His strong academic foundation and industry experience make him a reliable contributor to cutting-edge VLSI design projects.

ATAL FDP on "OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE"

Mr. Raja, Principal engineer @ Bay Area, USA

Mr. Raja is an accomplished Principal Engineer with 14 years of extensive experience in VLSI Backend Physical Design, currently based in the Bay Area, USA. Known for his expertise in delivering cutting-edge semiconductor solutions, he specializes in floor planning, placement, routing, timing closure, and design signoff for complex SOCs and ASICs. He completed M.Tech (Microelectronics and VLSI) from National Institute of Technology Durgapur and B.Tech (Electronics and Communication Engineering) from GMRIT.

Mr.P.Raviteja, Senior technical lead @ V Micron, Hyderabad.

Mr. P. Raviteja is a seasoned **VLSI Backend Physical Design Engineer** with **10 years of extensive experience** in delivering high-quality semiconductor solutions. Currently serving as a **Senior Technical Lead** at **V Micron**, Hyderabad, he specializes in managing and executing **end-to-end physical design flows**, including floor planning, placement, routing, timing closure, and signoff for complex SOCs and ASICs.

He holds a **B.Tech in Electronics and Communication Engineering (ECE)** from **Jawaharlal Nehru Technological University (JNTU)**, completed in 2014.

Mr. K.Uday ,Technical lead @ Intel, Bangalore

Mr. K. Uday is a proficient **VLSI Backend Physical Design Engineer** with **7 years of extensive experience** in semiconductor design and development. Currently working as a **Technical Lead** at **Intel**, Bangalore, he specializes in delivering complex physical design solutions, including floor planning, placement, SOCs and ASICs.

Mr. Uday holds an M.Tech and a B.Tech in Electronics and Communication Engineering (ECE) from Jawaharlal Nehru Technological University (JNTU).

ATAL FDP on "OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE"

ATAL Online 6 Day Faculty Development Programmes 2024-25 Schedule

FDP Thrust Area: Semiconductors

FDP Title: Outlook on best practices and strategies for chip design implementation - from Industry perspective

Start Date: 16/12/2024 **End Date: 21/12/2024,**

Day 1	Day 2	Day 3	Day4	Day 5	Day 6
6:00PM to 6:30PM	6:00PM to 6:30PM	6:00PM to 6:30PM	6:00PM to 6:30PM	6:00PM to 6:30PM	2:00PM to 3:30PM
Inaugural Session	**Session 3**	**Session 5**	**Session 7**	**Session 9**	**Session 11**
	Topic: Static Timing Analysis Name of the Expert: Sri Sujan K Designation & Organization: Founder, Tech Expert, Enium – Semiconductor, Bangalore, Years of Exp: 8	Topic: Synthesis Name of the Expert: Ms. Rashmi K Designation & Organization: Lead soc - Sr Lead Engineer, Intel-Bangalore, Years of Exp: 4	Topic: PD and Packaging Name of the Expert: Sri Uday K Designation & Organization: Technical Lead, Intel-Bangalore, Years of Exp: 7	Topic: Design For Testability Name of the Expert: Sri Hari T Designation & Organization: Lead Engineer Quest Global - Vizag, Years of Exp: 4	Topic: Digital Design & Verification Name of the Expert: Sri Raja Designation & Organization: Principal Engineer, Synopsys, Bay Area, USA. Years of Exp: 14
6:30PM to 8:00PM	7:30PM to 9:00PM	7:30PM to 9:00PM	7:30PM to 9:00PM	7:30PM to 9:00PM	3:30PM to 5:00PM
Session 1	**Session 4**	**Session 6**	**Session 8**	**Session 10**	**Session 12**
Topic: RTL-GDSII Name of the Expert: Sri Dilip Yenni Designation & Organization: Technical Manager, Quest Global-Hyderabad, Years of Exp: 10	Topic: Static Timing Analysis Name of the Expert: Sri Sujan K Designation & Organization: Founder, Tech Expert, Enium – Semiconductor, Bangalore, Years of Exp: 8	Topic: Placement & Routing Name of the Expert: Sri E Uday Kumar Designation & Organization: Sr Engineer, Tessolve Semiconductors, Banglore Years of Exp: 5	Topic: PD and Packaging Name of the Expert: Sri Uday K Designation & Organization: Technical Lead, Intel-Bangalore, Years of Exp: 7	Topic: Design For Testability Name of the Expert: Sri Hari T Designation & Organization: Lead Engineer Quest Global - Vizag, Years of Exp: 4	Topic: Digital Design & Verification Name of the Expert: Sri Raja Designation & Organization: Principal Engineer, Synopsys, Bay Area, USA. Years of Exp: 14
8:00PM to 9:30PM					5:00PM to 7:30PM
Session 2					**Session 13**
Topic: RTL-GDSII Name of the Expert: Sri Dilip Yenni Designation & Organization: Technical Manager, Quest Global-Hyderabad, Years of Exp: 10					Topic: Custom Layout Design Name of the Expert: Sri P Ravi Teja Designation & Organization: Sr Tech Lead, V Micron - Hyderabad, Years of Exp: 10
					6:30PM to 7:30PM **Online test & feedback**
					7:30PM to 8:00PM **Valedictory Session**

ATAL FDP on "OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE"

The inaugural session of the Faculty Development Program (FDP) titled "Outlook on Best Practices and Strategies for Chip Design Implementation - From Industry Perspective" was held online on 16th December 2024 at 6:00 PM. This session marked the beginning of an insightful and informative series focused on advancing knowledge in chip design.

The session commenced with a warm welcome to all participants by the **FDP Coordinator, Prof. S. Krishna Veni**, who introduced the theme of the FDP and outlined its significance in today's fast-evolving chip design industry. Prof. Veni emphasized the importance of understanding the latest strategies and best practices that drive innovation and excellence in chip design.

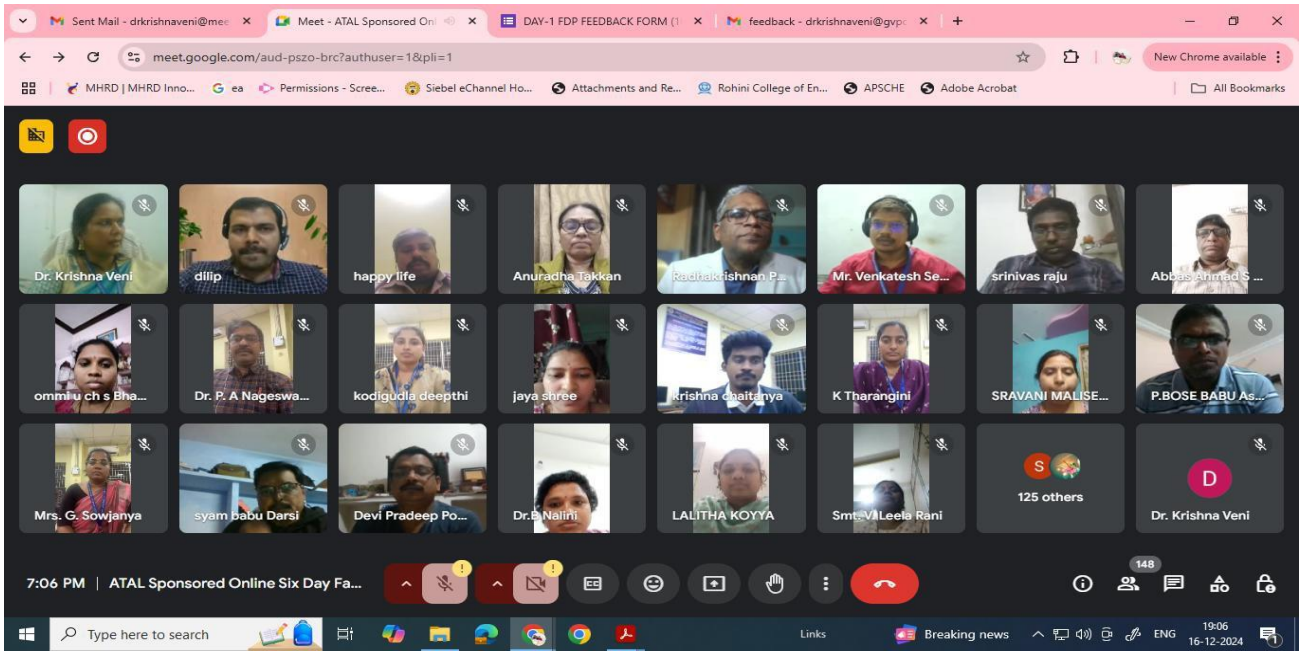
The chief guest for the inaugural session, **Dr. Radhakrishnan Pasirajan**, former scientist at **ISRO** and **Principal Director of E&T Programs**, delivered an enlightening speech. Dr. Pasirajan shared his extensive experience and insights from the industry, discussing the various challenges and innovations in the chip design domain. He emphasized the role of continuous learning and industry-academia collaboration in shaping the future of chip design. His address set the tone for the program, motivating the participants to engage actively and make the most of the knowledge shared during the FDP.

The **Principal, Prof. K.S. Bose**, also addressed the participants during the inaugural session. In his speech, Prof. Bose congratulated the participants for their commitment to professional development and encouraged them to apply the knowledge gained during the FDP to improve their skills and contribute to advancements in the field of chip design. His words were a source of inspiration for all present, reinforcing the importance of professional growth and continuous learning.

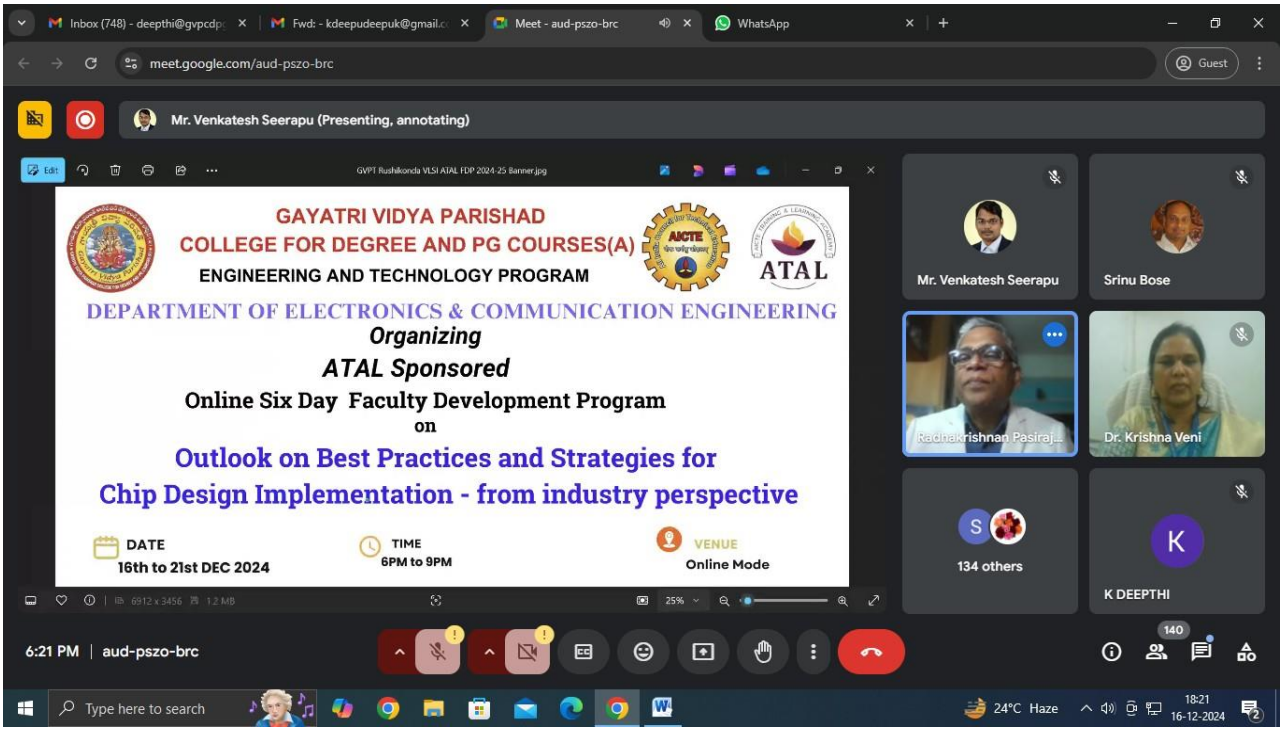
The session concluded with a vote of thanks by **Mr. S. Venkatesh**, the **FDP Co-Coordinator**. Mr. Venkatesh expressed gratitude to the chief guest, the principal, and all the participants for their presence and active involvement. He highlighted the importance of the topics to be covered in the upcoming sessions and encouraged participants to engage in meaningful discussions throughout the FDP.

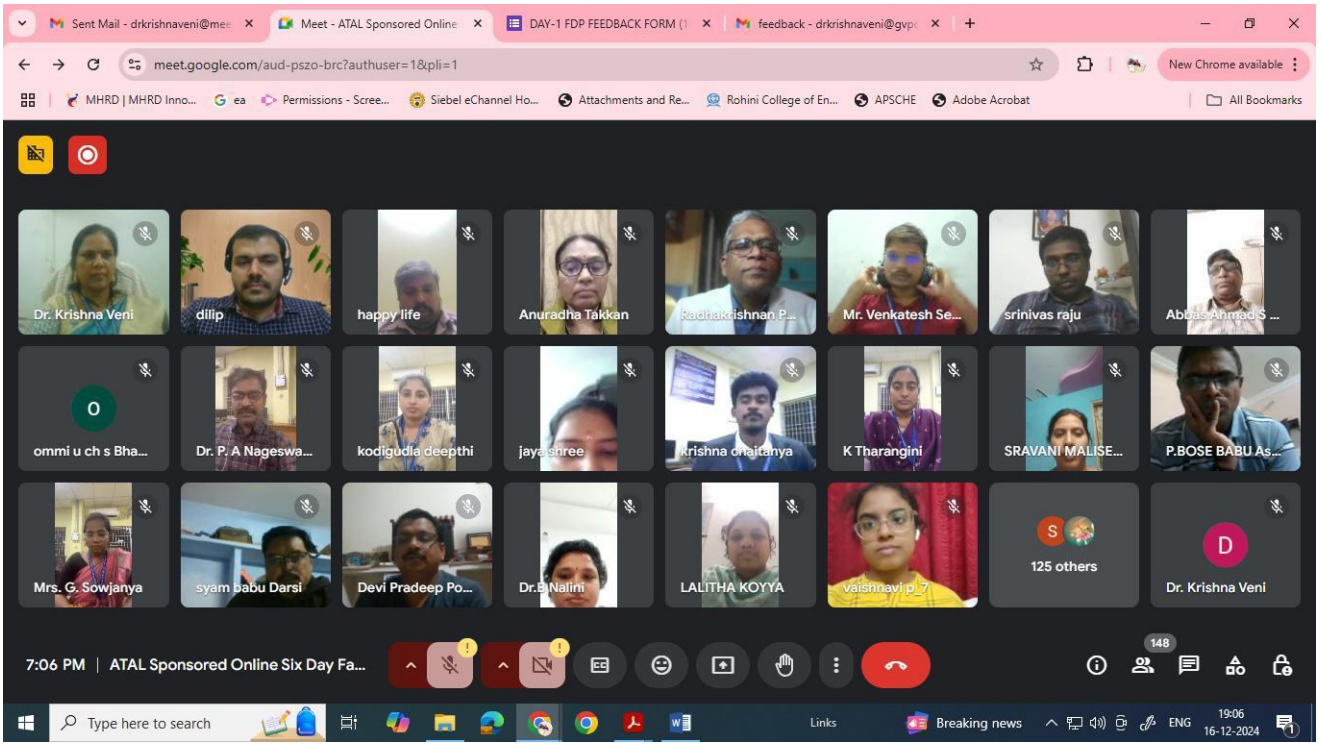
The inaugural session set the stage for a successful and enriching FDP, which promises to provide valuable insights into the best practices and strategies for chip design implementation from an industry perspective.

Screen shots of the Inaugural Session:



ATAL FDP on "OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE"





ATAL FDP on "OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE"

The list of participants are-

S. No	Name	Email	Phone	Institute Name	Designation
1	Dr. M. Jasmin	rifriz@gmail.com	9445240930	New Prince Shri Bhavani college of Engineering and Technology	Associate Professor
2	Dr. Rakesh Mutukuru	rakeshmmutukuru@gmail.com	9000454860	RISE Krishna Sai Prakasam Group of Institutions	Associate Professor
3	Dr. singam aruna	aruna9490564519@gmail.com	9705007304	Andhra University college of Engineering(A)	Associate Professor
4	Dr. S.RAMA DEVI	ramadevicf@andhrauniversity.edu.in	9491916090	ANDHRA UNIVERSITY	Assistant Professor
5	Mr. SHAIK IDRISH	idrish.shaik@becbapatla.ac.in	8309537934	Bapatla Engineering College	Assistant Professor
6	Mr. P DEVI PRADEEP	devipradeep.ece@anits.edu.in	9440399180	ANIL NEERUKONDA INSTITUTE OF TECHNOLOGY AND SCIENCES	Assistant Professor
7	Mr. GURJU MUNIRATHNAM	munirathnam.ece@jntua.ac.in	9966418874	JNTUACEK,KALIKIRI	Assistant Professor
8	Mr. SAI SUDHEER KOTTA	saisudheer1978@gmail.com	9849363769	SRI VASAVI INSTITUTE OF ENGINEERING & TECHNOLOGY	Assistant Professor
9	Mr. Sridhar Done	sridhar.done@gmail.com	9866612112	Sri Vasvi Institute of Engineering and Technology	Associate Professor
10	Dr. S M K M ABBAS AHMAD	smkmabbassrf@gmail.com	8985042004	Guru Nanak Institutions Technical Campus	Professor
11	Mr. Rallapati Aditya	r.adityace@gmail.com	7416482213	GITAM Deemed to be University	Assistant Professor
12	Mr. SAMMETA GOPI KRISHNA	gopi.krishna782@gmail.com	7842878200	GITAM (DEEMED TO BE UNIVERSITY)	Assistant Professor
13	Dr. SRINIVAS SABBAVARAPU	ssrinivas.ece@anits.edu.in	9989239486	Anil Neerukonda Institute of Technology and Sciences, UGC Autonomous	Associate Professor
14	Mr. Janamani Chandram Ayyangalam	janamani.chandram@gmail.com	9652123223	GITAM	Assistant Professor

15	Mr. SYAMBABU DARSI	syambabu.darsi@gmail.com	7680007684	RISE KRISHNA SAI PRAKASAM GROUP OF INSTITUTIONS	Associate Professor
16	Mrs. A.SUJATHA PRIYADHARSHINI	sujathabe08@gmail.com	9487294307	Parisutham Institute of Technology and Science	Assistant Professor
17	Mr. Pudu Atchutarao	apudu@gitam.edu	9703738767	Gitam deemed to be university	Faculty members of the AICTE approved institutions
18	Mr. VOLLURU MUTYALA NAIDU	vmn90gvd@gmail.com	9505052599	GAYATRI VIDYA PARISHAD COLLEGE FOR DEGREE AND PG COURSES(A)	Assistant Professor
19	Mr. CHANDRA KIRAN PATRUDU B	kiranec121@gmail.com	9985692690	ANDHRA UNIVERSITY COLLEGE OF ENGINEERING	Research Scholar
20	Mr. Siva Kumar	askshiva20@gmail.com	8179339880	anil neerukonda institute of Technology and sciences	Assistant Professor
21	Mr. KOLLABATHULA SURESH KUMAR	heartsuresh2004@gmail.com	9490230387	CHAITANYA ENGINEERING COLLEGE	Assistant Professor
22	Mrs. Pothala Chaya Devi	chayadevi.ece@anits.edu.in	9642289117	Anil Neerukonda Institute of Technology and Sciences	Assistant Professor
23	Dr. Murugapandiyan P	murugavlsi@gmail.com	8459633255	Anil Neerukonda Institute of Technology and Sciences	Associate Professor
24	Mr. Gudivada manikanta	manikantaecewstm@gmail.com	9640768681	WELLFARE INSTITUTE OF SCIENCE, TECHNOLOGY AND MANAGEMENT	Faculty members of the AICTE approved institutions
25	Mrs. Chavvakula Janaki Devi	ece2_hod@acet.ac.in	8008122280	Aditya College of Engineering and Technology	Faculty members of the

					AICTE approved institutions
26	Mr. PARISA.BOSEBABU	pbosebabu@aliet.ac.in	9440729045	ANDHRA LOYOLA INSTITUTE OF ENG.& TECH.	Assistant Professor
27	Mrs. padmasree challa	padmasreechalla8@gmail.com	9949345579	ANITS	Assistant Professor
28	Mrs. Mrs Nitya kanakamedala	nitya.kanakamedala@giet.edu	9182616668	Usharama college of engineering and technology	Assistant Professor
29	Mrs. GAYATRI GORLE	gayatri.gorli@gmail.com	9100220070	ANITS	Assistant Professor
30	Miss U.SIVARANJANI	usivaranjanisiva@gmail.com	7010712682	Parisutham Institute of Technology and Science	Assistant Professor
31	Mrs. jonnakuti nandini	jonnakutinandini456@gmail.com	8309973255	chaitanya engineering college	Faculty members of the AICTE approved institutions
32	Mr. C Bhargav	bargauv@gmail.com	8099078272	St John's college of Engineering and Technology	Assistant Professor
33	Mrs. JAYALAKSHMI YEDLA	jayashree959@gmail.com	9948619992	CHAITANYA ENGG COLLEGE	Faculty members of the AICTE approved institutions
34	Mr. B Venkatesh	venkatesh3813@gmail.com	9491993453	St John's College of Engineering & Technology, Yerrakota, Yemmiganur-518360	Assistant Professor
35	Mr. Chandra mouli Badithaboina	chandramouli.ece@anits.edu.in	9849065352	Anil neerukonda institute of technology and science	Assistant Professor
36	Dr. M Chandrasekhar	mc.ece@kitsw.ac.in	8374932535	kitsw	Assistant Professor

37	Mrs. sugandhi naidu Y	sugandhi.nusetti@gmail.com	7731915407	ADITYA UNIVERSITY	Faculty members of the AICTE approved institutions
38	Dr. Thota Vidyavathi	thota.vidyavathi9@gmail.com	8978882220	Anil Neerukonda Institute of Technology and sciences	Associate Professor
39	Mrs. K VIJAYA KUMARI	vijayakumarikala@gmail.com	9133618889	aditya college of engineering and technology	Faculty members of the AICTE approved institutions
40	Dr. AKASH KUMAR GUPTA	akgupta452@gmail.com	9490112550	Aditya University	Assistant Professor
41	Mr. RAJESH KATRAGADDA	katragaddarajesh@gmail.com	9885963630	NRI INSTITUTE OF TECHNOLOGY, AGIRIPALLI	Assistant Professor
42	Dr. R. M. JOANY	joany.ece@sathyabama.ac.in	9790902255	Sathyabama Institute of Science and Technology	Associate Professor
43	Mrs. EINDHUMATHY J	eindhumathy.j@gmail.com	9597544016	Saranathan college of Engineering	Assistant Professor
44	Dr. D Sreedevi	electronicssreedevi@gmail.com	9989590895	GVPCDPGC	Assistant Professor
45	Dr. Kusma Kumari Cheepurupalli	chkusumasrinivas@gvpce.ac.in	9703011760	Gayatri Vidya Parishad College of Engineering (A)	Associate Professor
46	Mr. K.Nataraju	knataraju@gvpcdpgc.edu.in	9985292574	GVP College for Degree and PG Courses(A)	Assistant Professor
47	Mr. SYED AHMED BASHA	ahmedbasha.syed@gmail.com	9985989634	St. John's college of eng.& tech.	Assistant Professor
48	Dr. Prasannakumar	prasanna.mani86@gmail.com	9994692826	Sri Ramakrishna College of Arts and Science	Assistant Professor
49	Mr. K S RAVI KUMAR	srinivas.ravikumar260@gmail.com	9866264335	Raghu Engineering College	Associate Professor
50	Dr. P A Nageswara Rao	panageswar@gmail.com	8328672542	Gayatri Vidya Parishad College for Degree and PG Courses	Associate Professor

51	Dr. Adinarayana	joy_adi2011@gmail.com	9441050887	GVP College for Degree and PG Courses(A)	Faculty members of the AICTE approved institutions
52	Mrs. Satya Sridevi B	sridevibaddireddy@yahoo.co.in	8790764777	Aditya Engineering College	Assistant Professor
53	Mr. RAMANA BABU CHALLAPALLI	ramana.challapalli86@gmail.com	9666191158	DADI INSTITUTE OF ENGINEERING AND TECHNOLOGY	Assistant Professor
54	Mr. Krishna Chaitanya	krishnachaitanyach4@gmail.com	8985367125	Gaytri Vidya parishad college for degree and pg courses	Assistant Professor
55	Mr. Veerraju Sampenga	sveerraju@diet.edu.in	7731925339	Dadi Institute of Engineering and Technology	Faculty members of the AICTE approved institutions
56	Mr. Mahesh Babu Ammisetty	maheshbabu07402@gvpcdpgc.edu.in	9059500989	Gayatri Vidya Parishad College for Degree and PG Courses (A)	Assistant Professor
57	Mr. Kasanagottu Srinivas	srinu.vasu11@gmail.com	9966118735	ST.PETER'S ENGINEERING COLLEGE	Assistant Professor
58	Miss KASI SATYA SHEELA	sheelaroy612@gmail.com	7893844107	aditya college of engineering and technology	Assistant Professor
59	Mr. VIJAY KUMAR GOPISETTI	gpvijay24@gmail.com	9949256432	St.Peters Engineering College	Assistant Professor
60	Miss Sandiri Swetha	swetha.sandiri@gmail.com	9603234508	St peters Engineering College	Faculty members of the AICTE approved institutions
61	Miss M Hamsalekha	hamsalekhamettu@gmail.com	7793932525	St.Peters Engineering college	Assistant Professor
62	Mrs. Phanimala Thiragati	phanimalathiragati@gmail.com	9502083533	Aditya College Of Engineering	Assistant Professor

63	Mr. NAVEEN S	snaveen@stpetershyd.com	8801804192	St.PETER'S ENGINEERING COLLEGE	Assistant Professor
64	Mr. G Ravi	ravi.gummula@gmail.com	9490140304	Visveraya college of engineering and technology	Assistant Professor
65	Miss Ganugapanta Anjana Harshitha Reddy	anjanaharshita5@gmail.com	8374622691	St.Peter's Engineering College	Assistant Professor
66	Mr. M RANJEETH REDDY	mranjithreddy@stpetershyd.com	9492428577	ST.PETER'S ENGINEERING COLLEGE	Assistant Professor
67	Mr. Kooram Praveen	praveenraj.kooram38@gmail.com	9666643862	st.peter's engineering college	Assistant Professor
68	Mrs. Veena Sanath Kumar	veenask7@gmail.com	9740080910	Acharya Institute of Technology	Assistant Professor
69	Miss Arelli Shruthi	arellishruthi@gmail.com	7893739263	St.Peter's Engineering College	Associate Professor
70	Mr. Raju Egala	402.raju@gmail.com	9966050337	Gayatri Vidya parishad college for Degree and PG Courses(A)	Faculty members of the AICTE approved institutions
71	Dr. V. LEELA RANI	lee_rani@gvpce.ac.in	9440366480	G.V.P College of Engineering(A)	Associate Professor
72	Mr. B SRAVAN KUMAR	sravanqisit@gmail.com	8143555994	St. PETER'S ENGINEERING COLLEGE	Faculty members of the AICTE approved institutions
73	Mrs. M Tharangini	mtharangini@gvpcdpgc.edu.in	9949609504	gayatri vidya parishad college for degree and PG courses (A)	Assistant Professor
74	Miss BEERA JAYA BHARATHI	jayabharathibeera@gmail.com	9573639357	St. PETER'S ENGINEERING COLLEGE	Assistant Professor
75	Mrs. P.N.S.SAILAJA	sailaja@sitam.co.in	9182817365	GAYATRI VIDYAPARISHAD COLLEGE FOR DEGREE AND PG COURSES	Assistant Professor

76	Dr. SaiTeja Chopparapu	saiteja.chopparapu960@gmail.com	9502462637	St. PETER'S ENGINEERING COLLEGE	Assistant Professor
77	Mrs. kodigudla deepthi	kdeepudeepuk@gmail.com	9705087904	GAYATRI VIDYA PARISHAD FOR DEGREE AND PG COURSES(A)	Assistant Professor
78	Mr. NADELLA CHENCHU CHANDU PRASANTH	chanduprasanthkvl@gmail.com	9494608935	St. Peter's Engineering College College , Hyderabad	Assistant Professor
79	Mrs. K Aruna Manjusha	22ecr1p06@gmail.com	9030917557	St. PETER's ENGINEERING COLLEGE	Assistant Professor
80	Mrs. Aruna Adlaboina	arunaece@gvpcdpgc.edu.in	7416267610	gayatri vidya parishad for degree and pg courses(A)	Assistant Professor
81	Mrs. velaga sridevi	sridevivelaga@gvpcdpgc.edu.in	9052294957	Gayatri vidya parishad for degree and pg courses(A)	Assistant Professor
82	Dr. S K GAYATRI DEVI	gayatrigavalapu@gmail.com	9490301962	Malla Reddy Engineering college	Faculty members of the AICTE approved institutions
83	Dr. Ch Manohar kumar	manohar.chebrolu@gmail.com	8143105787	Gayatri Vidya parishad college for degree and PG courses (A)	Associate Professor
84	Mrs. S.Madhavi	sangojumadhavi@gmail.com	7995857438	St. PETER'S ENGINEERING COLLEGE	Assistant Professor
85	Miss K MAHESWARI DEVI	kmaheswari820@gmail.com	9703700562	MALLA REDDY ENGINEERING COLLEGE SECUNDERABAD	Assistant Professor
86	Dr. Simasahu	drsimasahuece@gmail.com	8332908152	Malla Reddy Engineering College (Autonomous)	Associate Professor
87	Mr. KANDRAPU RAJESH KUMAR	krajeshkumar@lbce.edu.in	9701969560	Dr. Lankapalli Bullayya College of Engineering	Assistant Professor
88	Mr. PHANEENDRA KUMAR CH	phaneendra.chebrolu@gmail.com	9030626287	Malla Reddy University	Assistant Professor

89	Mr. Srinivasa Gupta Noolu	srinivasgupta.486@gmail.com	7036030777	RAGHU ENGINEERING COLLEGE	Assistant Professor
90	Dr. D.RAJA RAMESH	rajaramesh@mvgrce.edu.in	9573192720	MVGR COLLEGE OF ENGINEERING(A)	Associate Professor
91	Dr. MOHAMMAD HAYATH RAJVEE	razwe2003@gmail.com	9849825237	PBR VISVODAYA INSTITUTE OF TECHNOLOGY & SCIENCE	Professor
92	Dr. J NAVARAJAN	navarajan381@gmail.com	9884698433	PANIMALAR ENGINEERING COLLEGE	Associate Professor
93	Miss MADDIRALA SHILPA RAJ	mshilparaj@lbce.edu.in	8008265605	Dr Lankapalli Bullayya College OF Engineering	Assistant Professor
94	Mrs. suganthi T	suganthimanikandanpt@gmail.com	9597898245	P.S.V College of Engineering and Technology	Assistant Professor
95	Mrs. LALITHA KOYYA	lalitha.koyya@gmail.com	8121615387	Dr lankapalli bullayya college of engineering	Assistant Professor
96	Dr. Chandra Shankar	porwalchandra@gmail.com	8800959255	JSS Academy of Technical Education Noida	Associate Professor
97	Mrs. ANDIBOYINA VIJAYA SRI	avijayasri460@gmail.com	9704236432	Dr.Lankapalli bullaya college of engineering	Faculty members of the AICTE approved institutions
98	Mrs. JANANI M	mj.ece@builderscollege.edu.in	9047047363	Builders Engineering College	Assistant Professor
99	Mrs. OMMI U CH S BHAGYASRI	obhagyasri@lbce.edu.in	8019231091	DR LANKAPALLI BULLAYYA COLLEGE OF ENGINEERING	Assistant Professor
100	Mrs. sowjanya Lakshmi	sowjanya@gvpcdpgc.edu.in	9959062092	Gayatri vidya parishad college for Degree and PG Courses(A)	Assistant Professor
101	Mr. DOVA MURALI	murali.d@nriit.edu.in	9848506089	NRI INSTITUTE OF TECHNOLOGY	Associate Professor
102	Miss Kavya chalamalasetty	kavyachalamalasetty@gmail.com	9553465165	Sri vasavi engineering college	Assistant Professor
103	Mr. KONDETI CHOIRUNADH	chiru44817@gmail.com	8498012049	JNTUH COLLEGE OF ENGINEERING SULTANPUR	PG Scholars

104	Mrs. S ARUNA KUMARI	aruna0454@gmail.com	9493802085	RAGHU ENGINEERING COLLEGE (A)	Assistant Professor
105	Mr. ANEEL KUMAR RONGALI	rongali.aneel@gmail.com	9966669427	AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY	Assistant Professor
106	Mr. GUDLA BHANU GUPTA	bhanugupta407@gmail.com	9247282674	AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY	Assistant Professor
107	Mr. LOKARANJAN RAO PADALA	lokaranjanraopadala@gmail.com	9441789219	Avanti Institute of Engineering and Technology	Assistant Professor
108	Mrs. T L SPANDANA	spandanrm@gmail.com	8985353443	RAGHU ENGINEERING COLLEGE	Assistant Professor
109	Mrs. RAJALAKSHMI K	rajalakshmirathika98@gmail.com	9786643738	PANIMALAR ENGINEERING COLLEGE	Assistant Professor
110	Mr. BADUGU SANGEETA KUMAR	bskumar@lbce.edu.in	9160734644	DR.LANKAPALLI BULLAYYA COLLEGE OF ENGINEERING	Assistant Professor
111	Mrs. MALISETTY SRAVANI	sravanimalisetty02@gmail.com	7799138686	Dr LANKAPALLI BULLAYYA COLLEGE OF ENGINEERING	Assistant Professor
112	Dr. Gowri thumbur	gthumbur@gitam.edu	9441372387	Gitam university	Associate Professor
113	Dr. S. Neeraja	nsajja@gitam.edu	9985728450	GITAM Deemed to be University	Associate Professor
114	Mr. S S Kiran	sskiranece@gmail.com	8074527666	Lendi Institute of Engineering and Technology	Assistant Professor
115	Dr. G Manmadha Rao	profmanmadharao.ece@anits.edu.in	9441708119	Anil Neerukonda Institute of Technology & Sciences	Professor
116	Mrs. Epuri Deepthi	epurideepthi.406@gmail.com	7093169666	mrec	Research scholars
117	Mr. Santosh Tripurana	santoshtripurana@gmail.com	9949390106	Vignan's Institute of Engineering for women	Assistant Professor
118	Dr. K Renu	renucherry5214@gmail.com	9441162385	GITAM Deemed to be University	Assistant Professor
119	Mrs. U Geetalakshmi	geetaavanthiq7@gmail.com	7995376061	Avanthi Institute of engineering and technology	Assistant Professor
120	Mrs. Syamalakanchi mani	syamalanaac@gmail.com	9849591737	Avanthi Institute of engineering and	Faculty members of the

				technology, tagarapuvalasa, vzm	AICTE approved institutions
121	Dr. JAKUSANI SHIRISHA	drjshirisha@mrec.ac.in	9000358525	Malla Reddy Engineering College	Faculty members of the AICTE approved institutions
122	Dr. A CH SUDHIR	camanapu@gitam.edu	7660019088	GITAM (Deemed to be university)	Associate Professor
123	Mrs. GEETHA DUMPA	my.geetha@gmail.com	9494587520	AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY	Assistant Professor
124	Mrs. Ch Venkatalakshmi	venkatalakshmiavanthi@gmail.com	6309718019	Avanthi institute of Engineering &Technology	Assistant Professor
125	Mrs. Sowjanya Surampalli	sowji19.avanthi@gmail.com	9493821506	Avanthi Institute of engineering and technology	Assistant Professor
126	Mrs. K.Anuradha	anuradhatakkan@gmail.com	9441953007	Malla Reddy Engineering college (Autonomous)	Assistant Professor
127	Mr. JEYAKANNAN N	jeyakannan.n@gmail.com	9245190916	Panimalar Engineering College	Assistant Professor
128	Mrs. Karanam Uma Rani	kumarani@mrec.ac.in	7337200101	Malla Reddy Engineering College	Faculty members of the AICTE approved institutions
129	Miss MD.SHAMSHAD BEGUM	shamshad.ncet@gmail.com	9704071516	NIMRA COLLEGE OF ENGINEERING AND TECHNOLOGY	Assistant Professor
130	Mrs. Meegada Anusha	anusha.meegada@gmail.com	6300484969	vanthi Institute of Engineering and Technology	Assistant Professor
131	Dr. Chukka Rajasekhar	rchukka@gitam.edu	9989573144	GITAM (Deemed To Be University)	Assistant Professor
132	Dr. Venkata Rao Chalumuri	askvenkatarao@gmail.com	9492784784	Sanketika Vidya Parishad Engineering College, Visakhapatnam, A.P	Professor

133	Mrs. Lingam Sailaja	lingam.sailaja@gmail.com	9059815411	MREC(A)	Faculty members of the AICTE approved institutions
134	Mrs. PERAMBUDUR SOWJANYA	rishisowjanya@gmail.com	9701519851	MallaReddy Engineering College	Associate Professor
135	Mrs. Suneela	sunilareddyk@gmail.com	9948642316	malla reddy engineering college	Associate Professor
136	Dr. Nalini Bodasingi	nalinib.ece@jntukucev.ac.in	9912609545	JNTU GV	Assistant Professor
137	Mr. POTNURU NARAYANARAO	narayana1student@gmail.com	9000732479	Aditya Institute of Technology and Management	Assistant Professor
138	Dr. RAJU PALADUGU	rpaladug@gitam.edu	7794932159	GITAM Deemed to be University	Assistant Professor
139	Mr. Koteswararaonaik R	kramavat@gitam.edu	7893229439	gitam	Assistant Professor
140	Mr. Md Khwaja Muinuiddin Chisti	mchisti@gitam.edu	9573412381	GiTAM Deemed to be University, Visakhapatnam	Assistant Professor
141	Dr. NAGA RAJU KAKUMANU	nagaraju.kakumanu@becbapatla.ac.in	7993558711	Bapatla Engineering College	Faculty members of the AICTE approved institutions
142	Mr. GATRAM MAHESH	mahesh.gatram@becbapatla.ac.in	8096176479	Bapatla Engineering COllege	Faculty members of the AICTE approved institutions
143	Mrs. YARLAGADDA SRUTHI	ysruthi30@gmail.com	9030631990	BAPATLA ENGINEERING COLLEGE	Assistant Professor
144	Mrs. RAJITHA DATLA	rajitha.datla@gmail.com	9985239505	MIRACLE EDUCATIONAL SOCIETY GROUP OF INSTITUTIONS	Assistant Professor

145	Dr. K V RAMANA RAO	kvrrao@lbce.edu.in	9440974007	Dr. LANKAPALLI BULLAYYA COLLEGE OF ENGINEERING	Associate Professor
146	Mr. J. VENKATA SURESH	jvlithdev@gmail.com	8317624047	Miracle Educational Society group of institutions	Assistant Professor
147	Dr. MOUSUMI BHANJA	mousumi.bhanja@sitpune.edu.in	9434690379	SIT Pune	Faculty members of the AICTE approved institutions
148	Mrs. sailakshmi kumari narava	nslkumari@lbce.edu.in	7287918971	Dr.Lankapalli Bullayya College of Engineering	Faculty members of the AICTE approved institutions
149	Dr. Prasanna Kumar Korada	prasannakumar@stpetershyd.com	9533265962	St.Peter's Engineering College	Associate Professor
150	Mrs. Neeli Syamala	syamu.siri99@gmail.com	9949073369	St. Ann's college of Engineering & Technology	Assistant Professor
151	Mr. Venkatesh Seerapu	venkateshece@gvpcdpgc.edu.in	9666594294	Gayatri Vidya Parishad College for Degree and PG Courses	Assistant Professor
152	Dr. Sateesh Kumar Gudla	sateeshkumar.g@adityatekkali.edu.in	9440347764	Aditya Institute of Technology and Management	Professor
153	Mr. KURITI JOGINAIDU	k.joginaidu@cutmap.ac.in	7013737344	CENTURION UNIVERSITY AP CAMPUS	Assistant Professor
154	Mr. Balarama Murty Sannidhi	balaramamurty.ece@nsrit.edu.in	7989449720	NSRIT, VISAKHAPATNAM	Faculty members of the AICTE approved institutions
155	Mrs. D Nagamani	nagamani.ece@anits.edu.in	9491762858	ANITS	Assistant Professor
156	Mrs. Rayala Sree Varsha	sreevarsha2024@gmail.com	7643803699	VIT-AP	Student

157	Dr. Dr.Ch.Sumanth Kumar	schennup@gitam.edu	9885177336	Gandhi Institute of Technology and Management	Professor
158	Dr. Nutakki Jyothi	jnutakki@gitam.edu	9885362364	Gandhi Institute of Technology and Management	Associate Professor
159	Dr. Dunna Madhavi	mdunna@gitam.edu	7382733627	Gandhi Institute of Technology and Management	Associate Professor
160	Dr. RaviChandra Bandi	ravichand678@gmail.com	9866700873	N S Raju Institute of Technology(A), Visakhapatnam	Associate Professor
161	Mrs. Buditi Nagaratnam	smilypreeti20@gmail.com	9337394308	AITAM TEKKALI	Assistant Professor
162	Mr. Lingampally Shiv Prasad	ybplsp@gmail.com	9182422568	Kshatriya College of Engineering	Assistant Professor
163	Miss PAVITRA MODI	pavitra.m@visvodayata.ac.in	9493030178	PBRVITS	Faculty members of the AICTE approved institutions
164	Mrs. M.V.S.Roja Ramani	rojaramani.ece@nsrit.edu.in	9908019008	N S RAJU INSTITUTE OF TECHNOLOGY	Associate Professor
165	Mr. S SURESH KUMAR	sureshkumar62ssk@gmail.com	9963849797	Lendi Institute of Engineering and Technology	Assistant Professor
166	Mrs. KOTANA.YASHODA	yashoda.ece@anits.edu.in	9032609052	ANITS	Assistant Professor
167	Mrs. VANKA SHIREESHA	shireesha.ece@anits.edu.in	9963792396	ANIL NEERUKONDA INSTITUTE OF TECHNOLOGY & SCIENCES	Assistant Professor
168	Mrs. BANDARU NALINI SANTHOSHI RANI	bnsantoshirani.ece@nsrit.edu.in	9848650756	NADIMPALLI SATYANARAYANA RAJU INSTITUTE OF TECHNOLOGY	Assistant Professor
169	Mr. G DURGA PRASAD	durgaprasad.ece@nsrit.edu.in	9121735096	NADIMPALLI SATYANARAYANA RAJU INSTITUTE OF TECHNOLOGY	Assistant Professor
170	Miss Yerramsetti Manasa	manasa99yerramsetti@gmail.com	8919356732	Dr L bullayya college of engineering	Assistant Professor

171	Mrs. Velaga Suryakala	velagasuryakala@gmail.com	9542999192	Sankethika Vidya Parishad Engineering College	Faculty members of the AICTE approved institutions
172	Mrs. INDIRA DEVI GEDELA	gedela.indira@gmail.com	9676867978	ANIL NEERUKONDA INSTITUTE OF TECHNOLOGY AND SCIENCES	Assistant Professor
173	Dr. Sabbavarapu Saradha Rani	ssabbava@gitam.edu	9440399523	GITAM Institute of Technology, GITAM(Deemed to be University)	Assistant Professor
174	Mrs. Gayatri Allu	gayatriallu@gmail.com	9640078955	GIT	Assistant Professor
175	Mr. SURYA P	suryame3020@gmail.com	9790714289	RISE KRISHNA SAI PRAKASAM GROUP OF INSTITUTIONS	Faculty members of the AICTE approved institutions
176	Mr. ADIL ZAIDI	er.adilzaidi@gmail.com	8826319440	MEWAT ENGINEERING COLLEGE, WAQF	Assistant Professor
177	Dr. Ratna Kumari Upadhyayula	rupadhya@gitam.edu	8885487159	GITAM	Assistant Professor
178	Mr. Ram Nishanth Vanka	ramnishanthvanka@gvpcdpgc.edu.in	9951407884	Gayatri Vidya Parishad College for Degree and PG Courses	Assistant Professor
179	Mr. Shaik Aktahar	athehar0@gmail.com	9398808161	VFSTR	Research scholars
180	Mrs. S S BHAVANI	srinu.mugandi@gmail.com	9966188432	Avanthi Institute of Engineering and Technology	Assistant Professor
181	Dr. ganesh laveti	ganeshlaveti2010@gvpcew.ac.in	9642306135	GVP College of Engineering for Women	Faculty members of the AICTE approved institutions

182	Mr. K. SANTHOSH KUMAR	ksanthoshtanjore@gmail.com	9843012785	parisutham Institute of technology and science	Assistant Professor
183	Mr. Tammineni Ravindra	ravindra@gvpce.ac.in	9440580583	GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING(AUTONOMOUS)	Assistant Professor
184	Dr. Rajasekhar Manda	raja.sekhar441@yahoo.co.in	7730984441	QIS College of Engineering and Technology (A)	Associate Professor
185	Mrs. KOLLI V JAYALAKSHMI	kvjlakshmi@lbce.edu.in	9247868888	Dr.Lankapalli Bullayya College of Engg	Assistant Professor

Day 1 Session 1 & Session 2:

Scaling Importance: VLSI scaling drives innovation in mobile devices, AI processors, and automotive electronics by increasing power efficiency and computational capacity.
Industry-Leading Companies: Apple, Qualcomm, AMD, Intel, Broadcom, Nvidia, and others play critical roles in advancing VLSI applications.
Technological Transition: The shift from MOSFET to FinFET is pivotal for meeting the demand for miniaturization and enhanced energy efficiency in modern electronics.

ASIC/SoC Flow Diagram:

- Depicts a step-by-step pipeline of the design process:
    1. **Chip Specification:** Defines functionality and performance.
    2. **Design Entry & Functional Verification:** Validates the design at the RTL level.
    3. **RTL Synthesis:** Converts RTL code into gate-level logic.
    4. **Partitioning of Chip:** Divides the chip into manageable sections.
    5. **Design for Test (DFT):** Adds testability features.
    6. **Floorplanning:** Organizes components for optimal performance.
    7. **Placement Stage:** Determines locations for various components.
    8. **Clock Tree Synthesis (CTS):** Ensures clock signals are distributed efficiently.
    9. **Routing Stage:** Establishes connections between components.
    10. **Final Verification:** Confirms design integrity before fabrication.
    11. **GDSII Generation:** Produces the final layout for manufacturing.

Company Roles and Ecosystem (Pyramid):

- The ecosystem for ASIC/SoC design and fabrication involves multiple stakeholders:
    - **Foundries:** Manufacture chips based on designs (e.g., TSMC, Samsung, GlobalFoundries).
    - **IDMs (Integrated Device Manufacturers):** Handle both design and fabrication (e.g., Intel, Texas Instruments).
    - **Fabless Companies:** Focus solely on design and rely on foundries for manufacturing (e.g., Nvidia, Qualcomm).
    - **Wafer Fab Equipment Providers:** Supply tools for fabrication (e.g., ASML).
    - **EDA (Electronic Design Automation) Software Tools:** Support design and layout (e.g., Cadence, Synopsys, Mentor Graphics).
    - **IP Core Providers:** Offer reusable blocks for faster design (e.g., ARM, Cadence).

Additional Considerations in the Flow

- **Power Analysis and Optimization**: Power analysis ensures the design operates within the power budget, often incorporating techniques like **clock gating** (turning off unused circuits) and **power gating** (powering down sections of the chip when idle).
- **Signal Integrity**: Ensuring that signals are transmitted without distortion, which might involve adding buffers, reducing wire length, or adjusting routing layers.
- **Timing Analysis**: Analyzing and ensuring that the design meets its timing constraints, ensuring that signals propagate through the circuit within required time limits.

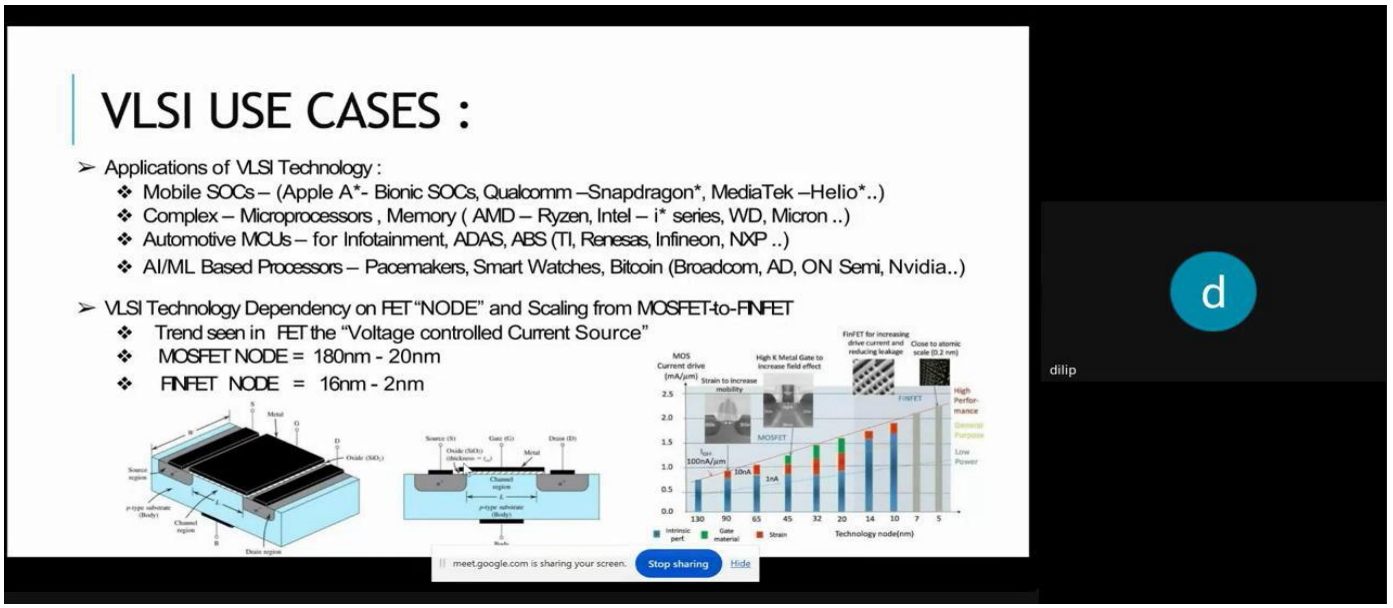
Tools and Methodologies

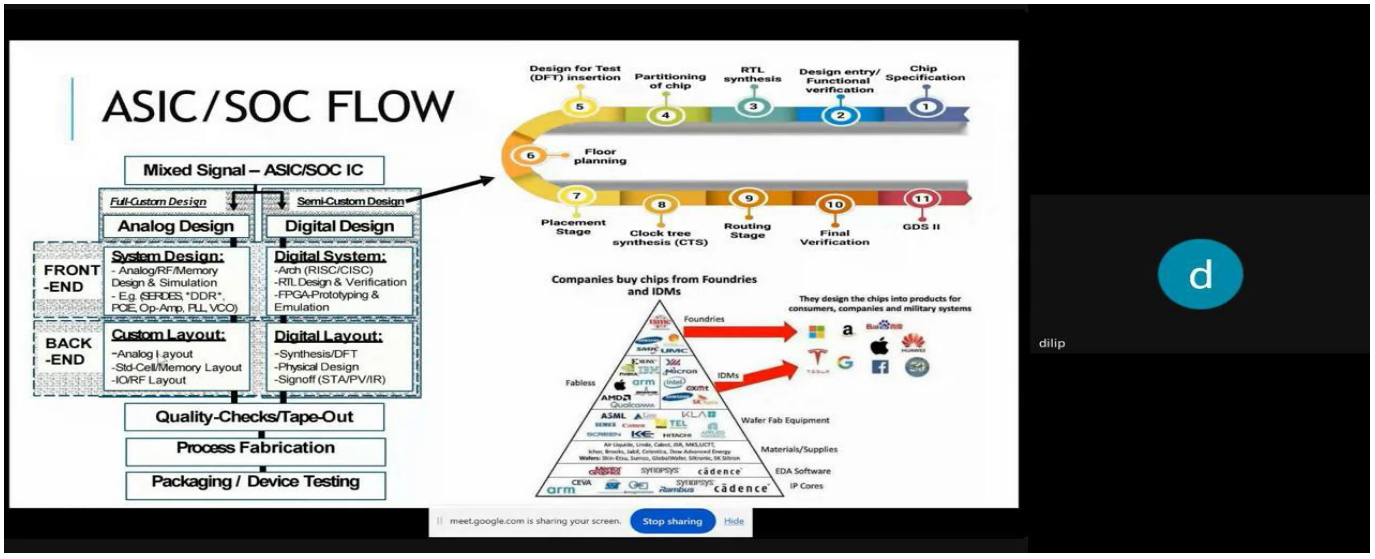
- Tools used in the RTL to GDSII flow include **Cadence**, **Synopsys**, and **Mentor Graphics** for synthesis, place and route, and verification.
- **FPGA Prototyping**: Some designs are first prototyped on **FPGAs** (Field Programmable Gate Arrays) before finalizing the GDSII layout, allowing for functional testing of the design before committing to silicon.

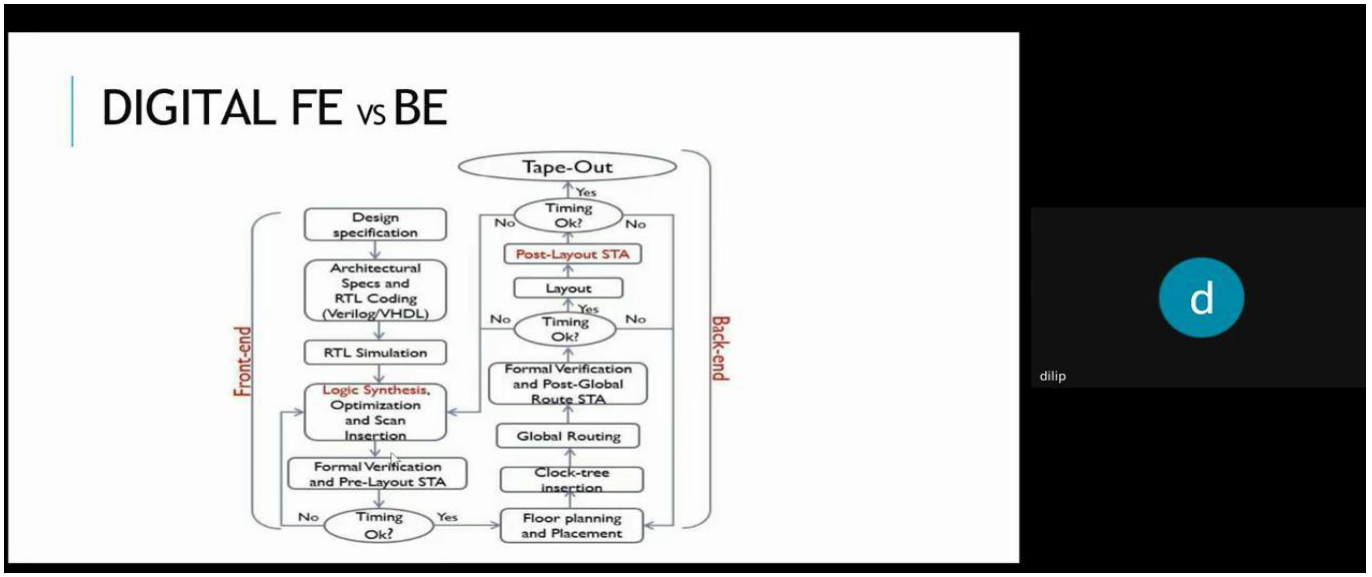
Importance

- This flow ensures that a high-level RTL design is translated into a manufacturable physical chip layout, meeting all performance, power, area, and timing specifications.
- It's critical for the successful development of complex ICs and SoCs used in smartphones, computers, and other electronic devices.

Screen Shots of Day 1 Session 1 & Session 2:







Day 2 Session 3 & Session 4:

Static Timing Analysis (STA) is a technique used in digital circuit design to verify the timing performance of a chip without requiring input test vectors. It is a critical step in the ASIC/SoC design process to ensure that a circuit meets its timing requirements and functions reliably at the intended clock speed.

Key Concepts in STA:

1. **Purpose:**
   - To ensure that all signal paths in a circuit meet the required timing constraints, such as setup time, hold time, and clock frequency.
2. **Key Timing Metrics:**
   - **Setup Time:** The minimum time before the clock edge that data must be stable.
   - **Hold Time:** The minimum time after the clock edge that data must remain stable.
   - **Clock Frequency:** Determines the maximum delay allowed in a path (clock period).
3. **Types of Timing Paths:**
   - **Combinational Paths:** Between two registers or inputs and outputs.
   - **Sequential Paths:** Include setup and hold checks at flip-flops or latches.
4. **Critical Path:**
   - The longest timing path in the circuit that determines the maximum clock frequency.
5. **Slack:**
   - The difference between the required time and the actual time for a signal to propagate.
   - **Positive Slack:** Indicates timing is met.
   - **Negative Slack:** Indicates a timing violation.

Steps in STA:

1. **Netlist Preparation:**
   - Uses a gate-level netlist generated from RTL synthesis.
2. **Constraint Application:**
   - Timing constraints are defined using a **Timing Constraint File** (e.g., SDC - Synopsys Design Constraints).
3. **Clock Tree Analysis:**
   - Clock paths are analyzed for skew and latency.
4. **Path Analysis:**
   - Checks all paths between source and destination for timing violations.
5. **Report Generation:**
   - Detailed reports on timing, slack, and violations.

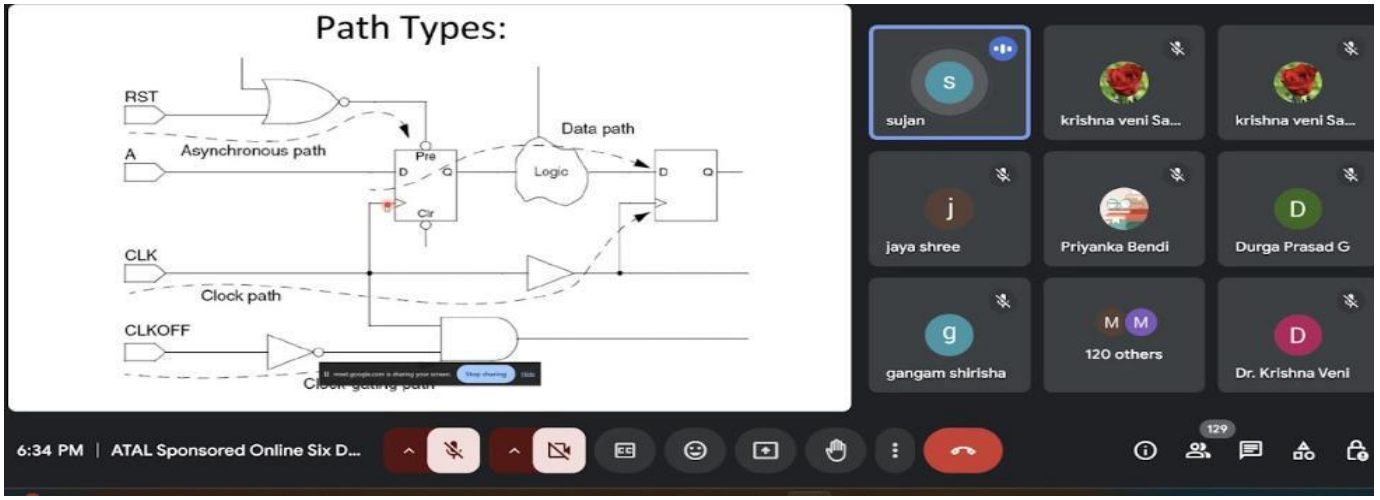
Advantages of STA:

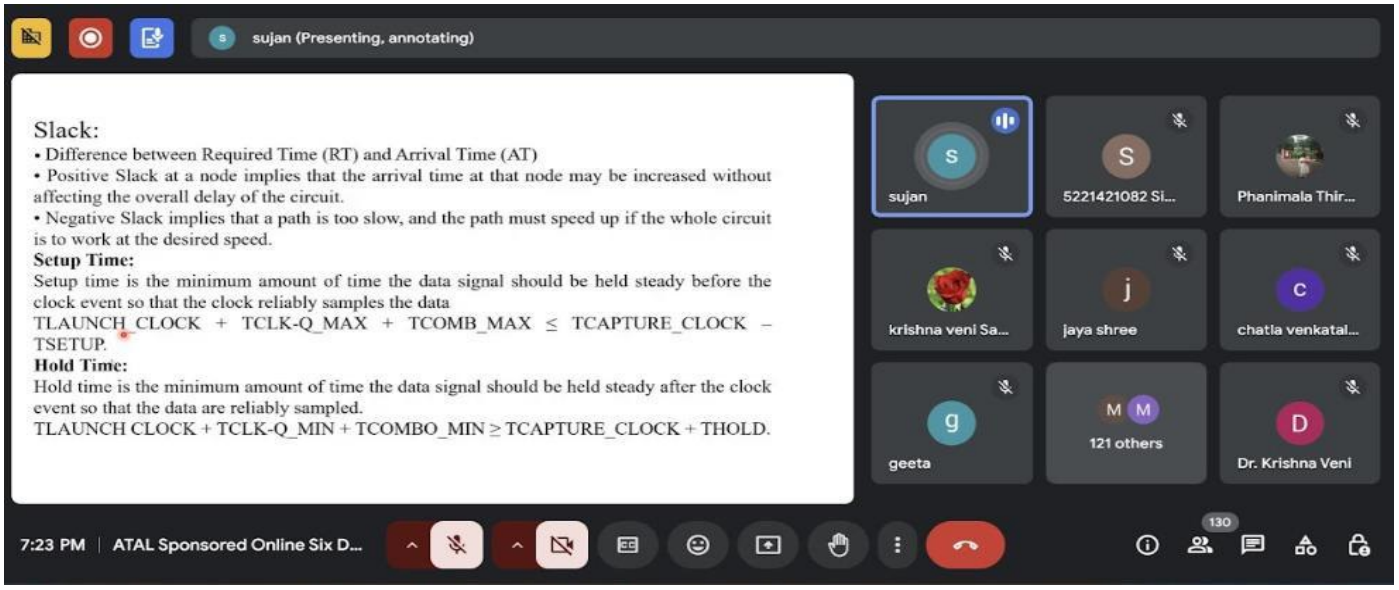
- **Vectorless Analysis:** No test vectors are required, making it faster than dynamic simulation.
- **Early Detection:** Identifies potential timing issues early in the design process.
- **Automation:** Compatible with EDA tools like Synopsys PrimeTime, Cadence Tempus, and Mentor Graphics TimeQuest.

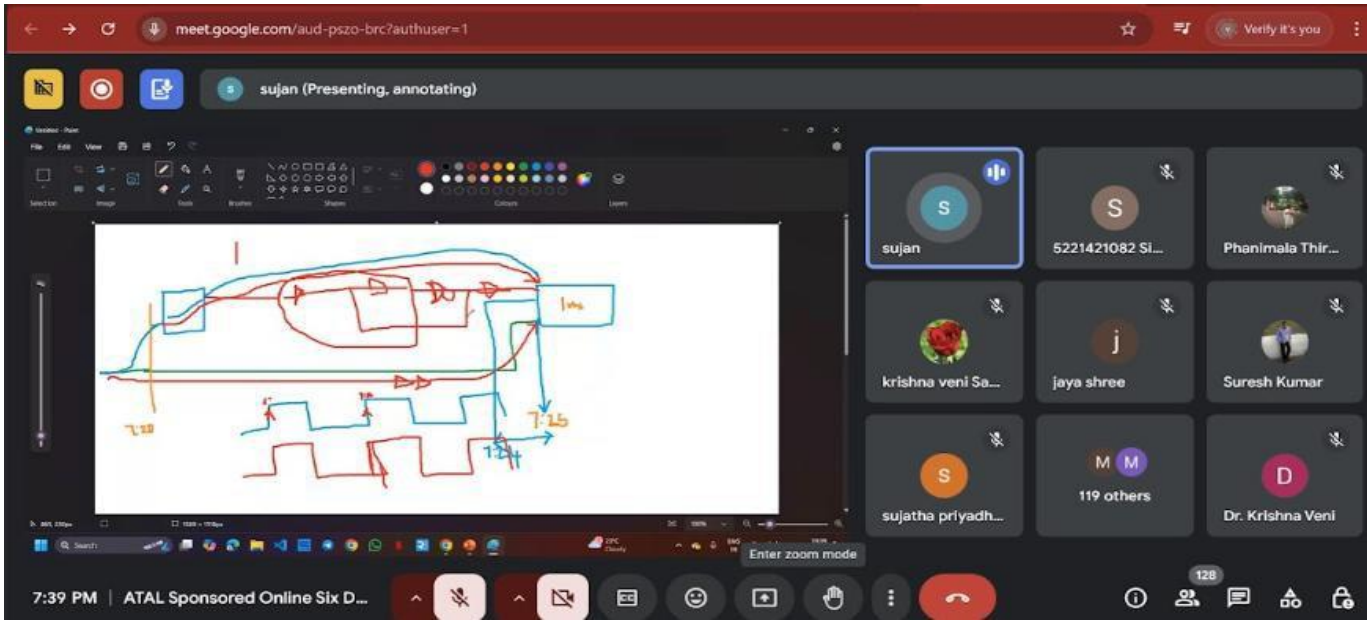
Challenges in STA:

- **Complexity:** Large designs can have millions of timing paths to analyze.
- **Process Variations:** Needs to account for variations in process, voltage, and temperature (PVT).
- **False/Multicycle Paths:** Requires accurate specification of exceptions to avoid unnecessary violations.

Screen Shots of Day 2 Session 3 & Session 4:







Day 3 Session 5:

Synthesis is the process of converting a high-level hardware description (written in languages like Verilog or VHDL) into a gate-level netlist that represents the circuit in terms of standard cells (e.g., logic gates, flip-flops) provided by the technology library. It bridges the gap between the **behavioral description** of a circuit and its **physical implementation**.

Key Goals of Synthesis:

1. **Translate RTL to Logic Gates:**
   - Transform Register-Transfer Level (RTL) code into a netlist of combinational and sequential logic gates.
2. **Optimization:**
   - Minimize area, power, and delay while meeting the functional and timing constraints.
3. **Constraint Fulfillment:**
   - Ensure that the synthesized design adheres to timing, power, and area constraints specified in the design constraints file.

Steps in the Synthesis Process:

1. **RTL Analysis:**
   - The RTL code is analyzed for syntax, semantics, and structural consistency.
2. **Logic Optimization:**
   - Simplifies the logic to reduce gate count, area, or power consumption while preserving functionality.
3. **Technology Mapping:**
   - Maps the optimized logic into the gates and cells available in the target technology library (e.g., NAND, NOR, flip-flops).
4. **Timing Analysis:**
   - Performs static timing checks to ensure that all timing constraints, such as setup and hold times, are met.
5. **Constraint Application:**
   - Uses a constraint file (e.g., SDC - Synopsys Design Constraints) to guide synthesis:
     - Timing constraints (clock definitions, delays).
     - Area constraints.
     - Power constraints.
6. **Netlist Generation:**
   - Produces a gate-level netlist that describes the circuit in terms of the standard cells.

Key Inputs for Synthesis:

1. **RTL Code:** Written in Verilog or VHDL.
2. **Technology Library:** Contains standard cells with their timing, power, and area characteristics.
3. **Constraints File (SDC):** Specifies design requirements like clock frequency, delays, and exceptions.
4. **EDIF Files:** Defines external I/O interfaces.

Outputs of Synthesis:

1. **Gate-Level Netlist:** Represents the design using standard cells.
2. **Timing Reports:** Summarize timing analysis results.
3. **Area and Power Reports:** Provide details on resource utilization.
4. **Warnings/Violations:** Highlight issues like unmet constraints or combinational loops.

Advantages of Synthesis:

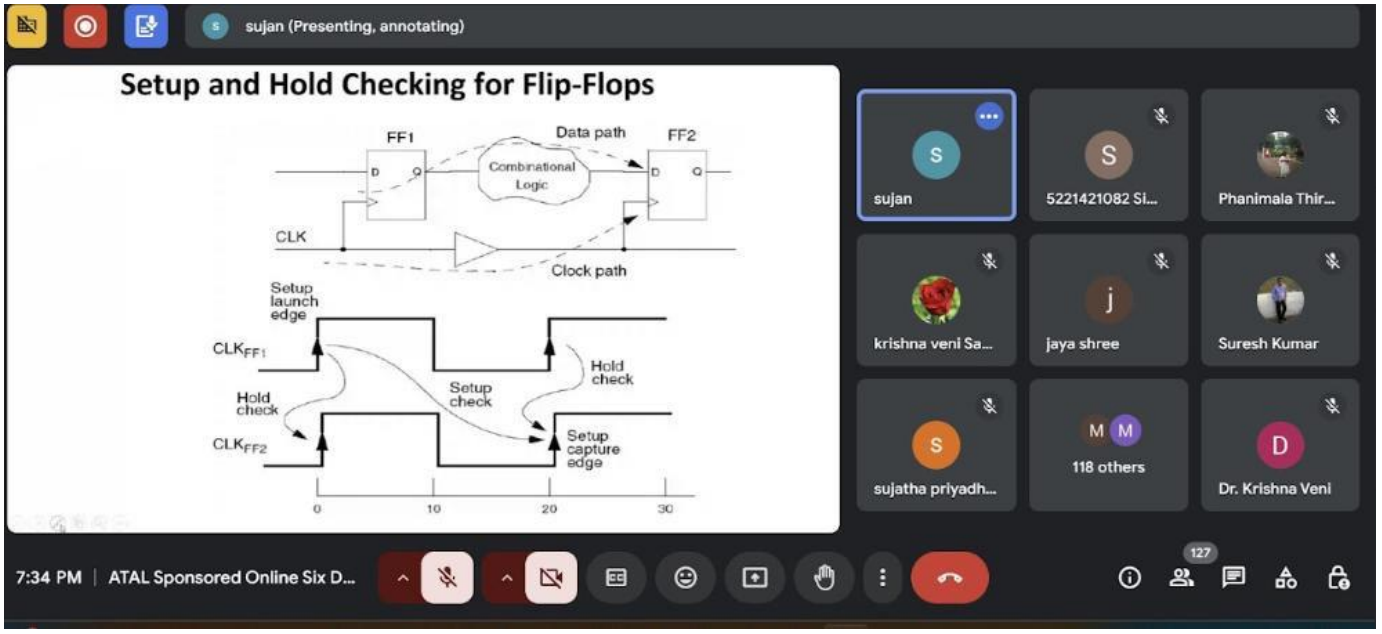
- **Automation:** Significantly reduces manual effort by automating logic design and optimization.

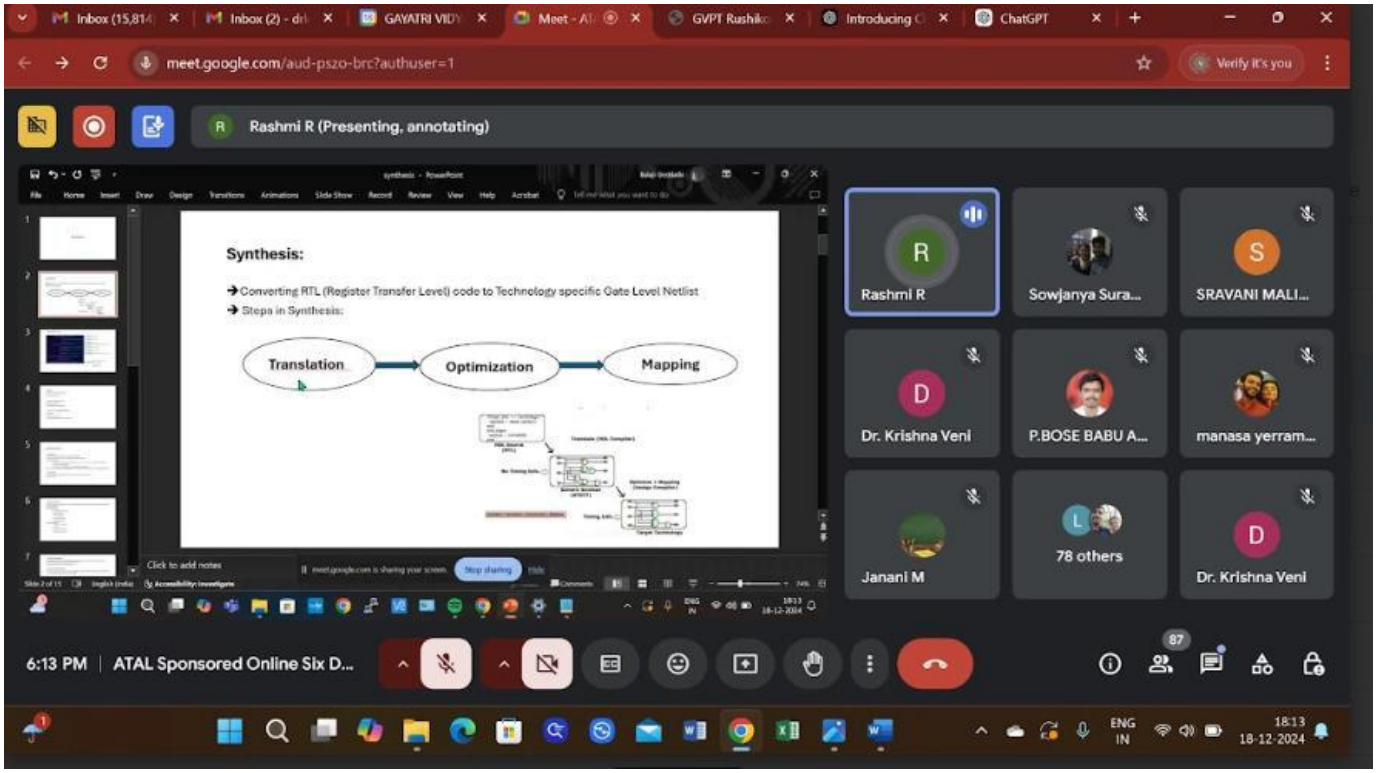
- **Optimization:** Balances competing design goals (performance, power, and area).
- **Scalability:** Handles large designs efficiently.

Challenges in Synthesis:

1. **Constraint Complexity:** Requires accurate and detailed constraints to ensure correct synthesis.
2. **Timing Closure:** Achieving timing goals can be difficult for high-frequency designs.
3. **Tool Dependency:** Relies on EDA tools like Synopsys Design Compiler, Cadence Genus, or Mentor Graphics Precision.

Screen Shots of Day 3 Session 5:





Day 3 Session 6:

Placement and Routing (P&R) are critical stages in the physical design of VLSI circuits. They involve arranging the synthesized standard cells and creating the interconnections (wires) between them to meet design constraints like timing, area, and power.

1. Placement

Purpose:

- **Placement** determines the optimal physical locations of standard cells, macros, and I/O pads on the chip layout.

Key Goals:

- Minimize wire length for efficient routing.
- Optimize for timing, area, and power.
- Avoid congestion and ensure thermal dissipation.

Steps in Placement:

1. **Global Placement:**
   - Determines approximate positions of cells to minimize timing delay and wire length.
2. **Legalization:**
   - Adjusts the cell locations to align with the grid and avoid overlaps.
3. **Detailed Placement:**
   - Refines the placement to further optimize timing and minimize cell movement.

2. Routing

Purpose:

- **Routing** connects the placed cells by creating physical wires for all signal nets.

Key Goals:

- Ensure all connections are completed without violations.
- Minimize delays, wire length, and power consumption.
- Avoid congestion and crosstalk.

Steps in Routing:

1. **Global Routing:**
   - Divides the chip into regions and determines approximate routing paths for each net.
2. **Detailed Routing:**
   - Specifies the exact routing paths within each region, considering the metal layers and design rules.
3. **Final Routing:**
   - Resolves any violations and optimizes the final routing layout.

Key Challenges in P&R:

1. **Congestion:**
   - Overlapping or excessively dense routes can lead to routing failures.
2. **Timing Closure:**
   - Ensuring all timing paths meet the setup and hold time requirements post-routing.
3. **Crosstalk and Noise:**
   - Avoiding interference between closely placed wires.
4. **Design Rule Violations (DRVs):**
   - Ensuring adherence to foundry-specific design rules for routing.

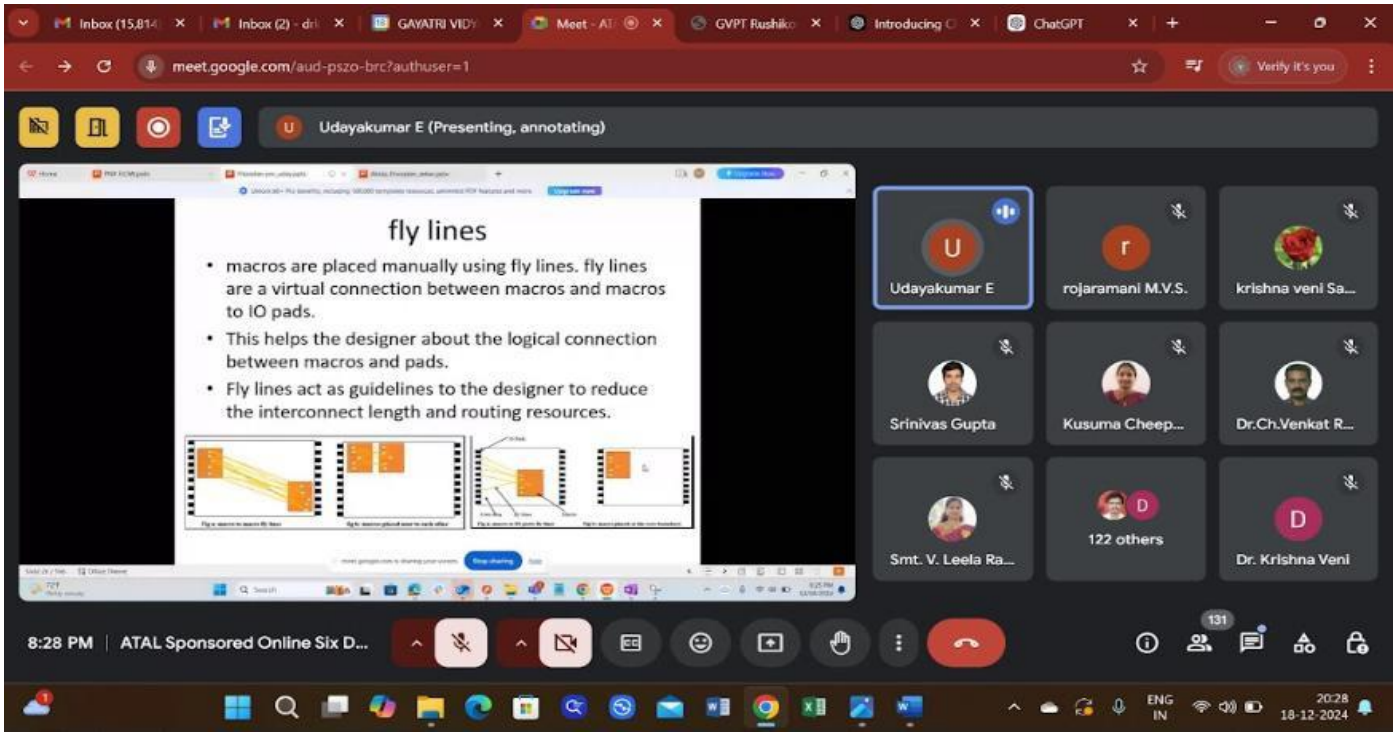
Outputs of P&R:

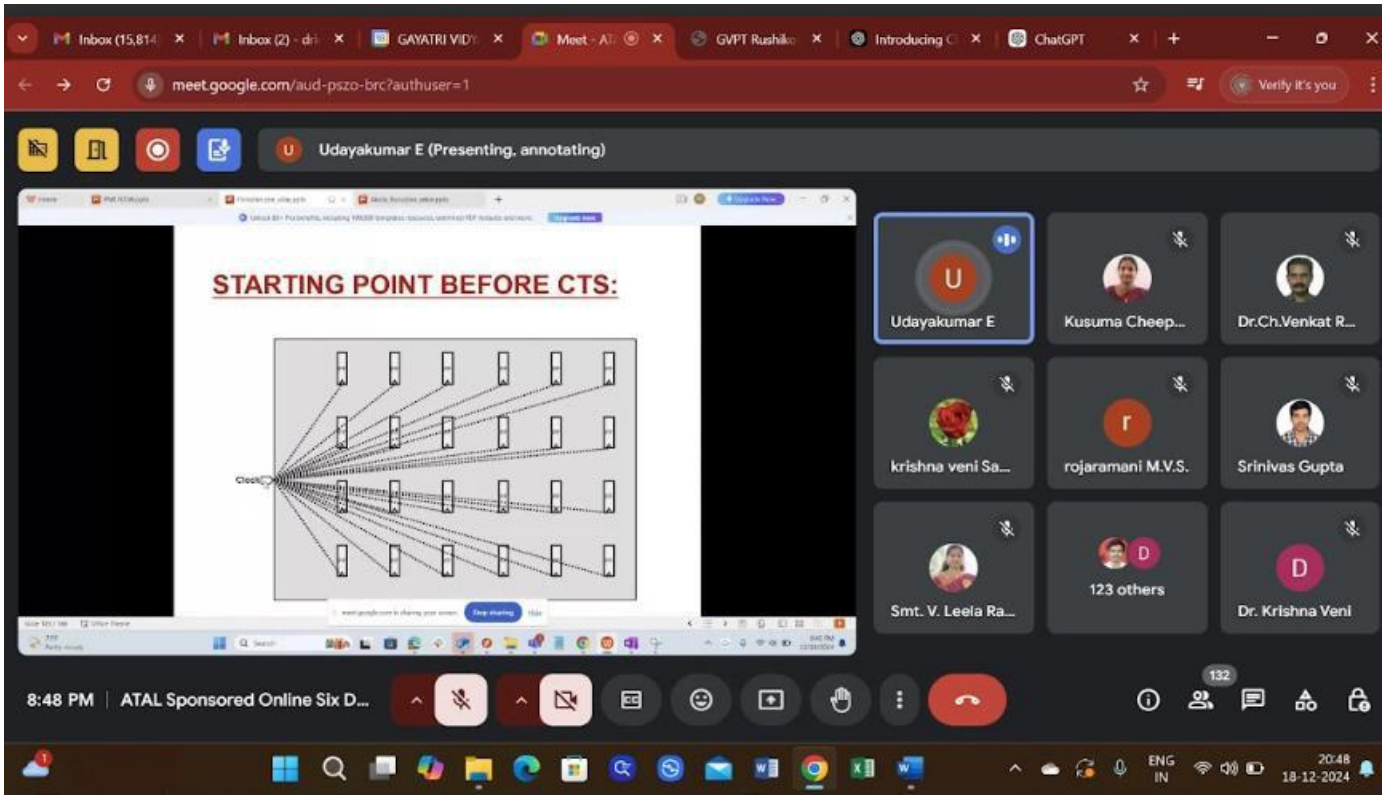
1. **Placed Layout:**
   - A physical representation of the cell locations on the chip.
2. **Routed Netlist:**

- A detailed list of connections between cells with exact routing paths.

3. **Timing Reports:**
   - Analyze any timing violations introduced during placement and routing.
4. **Parasitic Extraction (SPEF/RC):**
   - Provides parasitics (resistance, capacitance) for timing analysis.

Screen Shots of Day 3 Session 6:





Day 4 Session 7 & Session 8:

Physical Design and **Packaging** are essential steps in the back-end flow of VLSI design. These stages translate the logical design into a manufacturable layout and prepare the chip for integration into electronic systems.

1. Physical Design

Physical Design is the process of transforming a gate-level netlist into the physical layout of a chip that adheres to manufacturing constraints.

Key Steps:

1. **Floor planning:**
   - Arranges macros, standard cells, and I/O pads on the chip.
   - Defines chip dimensions, power grid structure, and placement regions.
   - Goals: Optimize area utilization and facilitate effective routing.
2. **Power Planning:**
   - Creates a power distribution network (PDN) to deliver power to all cells with minimal IR drop and noise.
3. **Placement:**
   - Determines the exact locations of standard cells and macros on the chip, minimizing wire length and optimizing timing.
4. **Clock Tree Synthesis (CTS):**
   - Designs a clock distribution network to minimize skew and latency, ensuring synchronized operation across the chip.
5. **Routing:**
   - Connects cells and macros using metal layers while adhering to design rules.
   - Steps: Global routing, detailed routing, and final routing.
6. **Design Rule Checking (DRC) & Layout vs. Schematic (LVS):**
   - Verifies that the layout complies with manufacturing rules and matches the logical design.
7. **Parasitic Extraction:**
   - Calculates parasitic resistances and capacitances for accurate timing and power analysis.
8. **Timing Closure:**
   - Ensures that all timing paths meet the setup and hold time requirements after placement, CTS, and routing.

2. Packaging

Packaging involves enclosing the fabricated chip in a protective casing that provides electrical connections, thermal management, and mechanical stability.

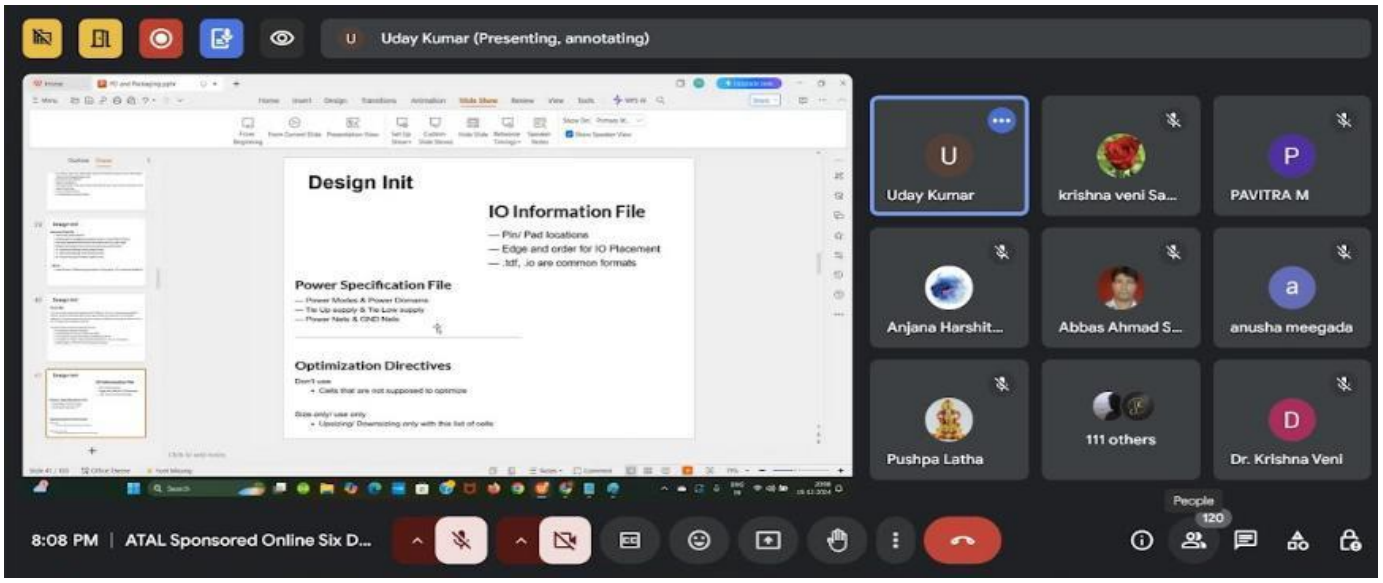
Key Functions:

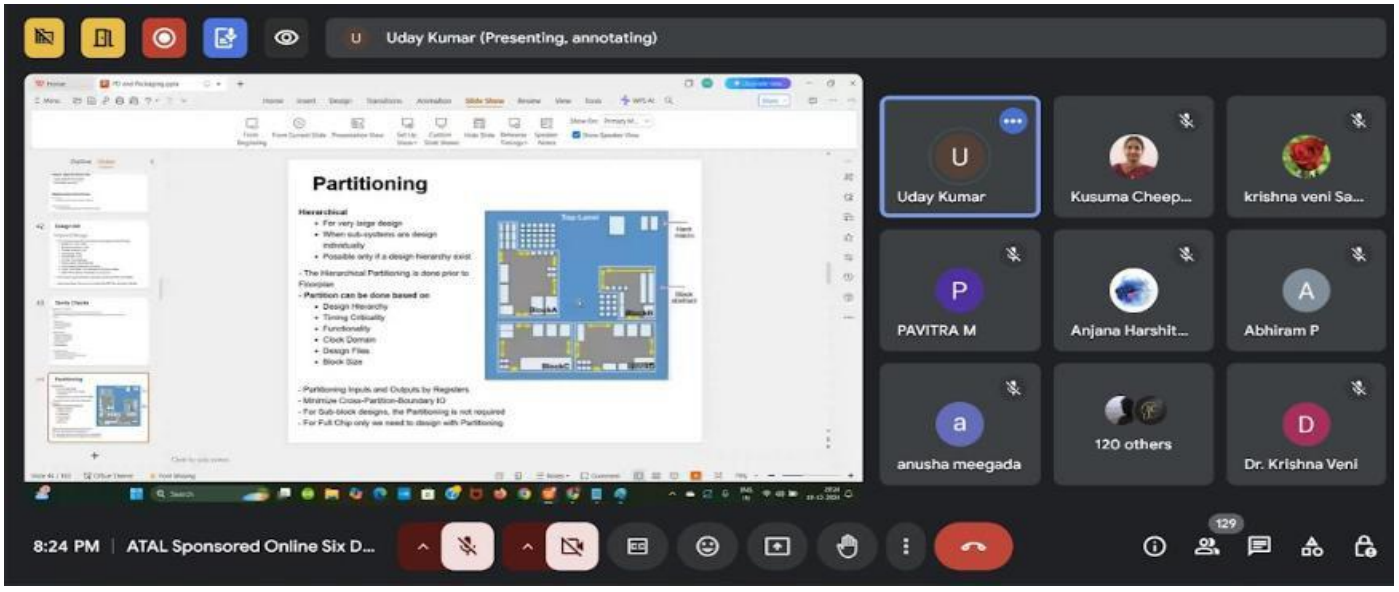
- Protect the chip from environmental factors like moisture, dust, and physical damage.
- Provide electrical connectivity between the chip and the circuit board.
- Dissipate heat generated by the chip during operation.

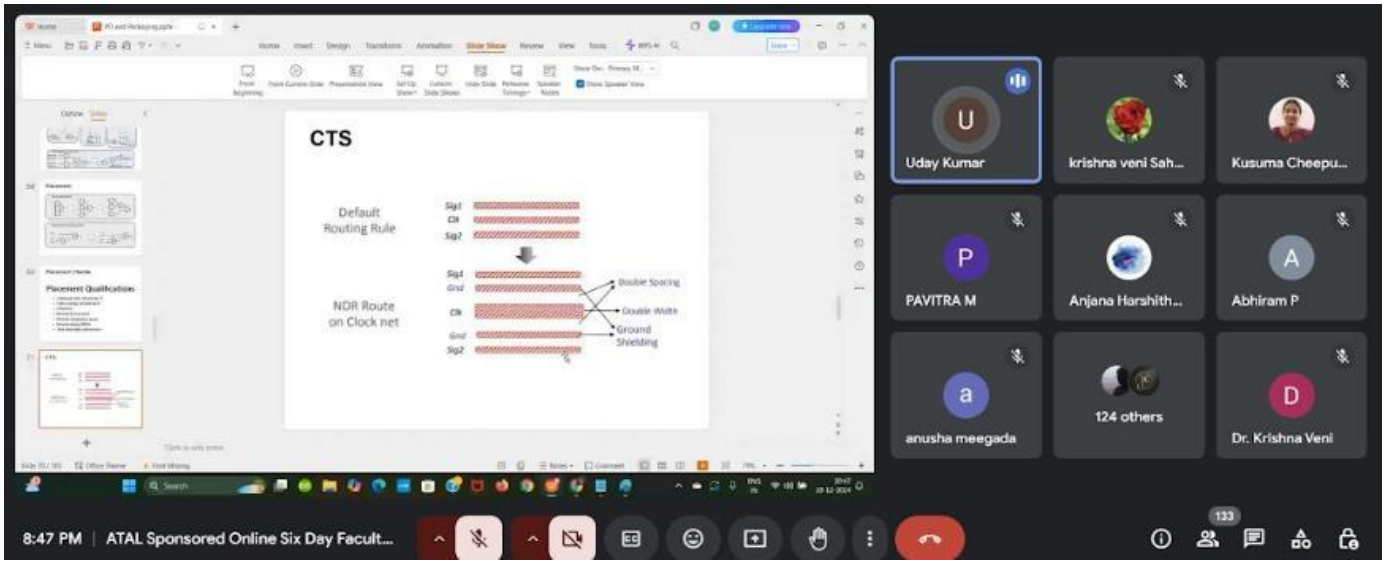
Types of Packaging:

1. **Wire Bonding:**
   - Connections are made using thin wires from the chip to the package leads.
   - Common in low-cost and low-performance applications.
2. **Flip-Chip Packaging:**
   - Solder bumps are used to directly connect the chip to the package substrate.
   - Preferred for high-performance and high-density designs.
3. **System-in-Package (SiP):**
   - Integrates multiple chips or components into a single package.
   - Used in applications requiring high integration and miniaturization.
4. **3D Packaging:**
   - Stacks multiple chips vertically to reduce form factor and improve performance.

Screen Shots of Day 4 Session 7 & Session 8:







Day 5 Session 9 & Session 10:

Design for Testability (DFT) is a methodology used in VLSI design to ensure that manufactured chips can be effectively tested for defects and faults. Since modern ICs are highly complex, DFT techniques are essential to identify and isolate manufacturing defects, ensuring high-quality and reliable chips.

Goals of DFT:

1. **Enhance Test Coverage:** Maximize the ability to detect manufacturing defects in logic, interconnects, and memories.
2. **Minimize Test Time and Cost:** Simplify test generation and reduce testing overhead.
3. **Ensure Fault Isolation:** Enable identification of defective components within the chip.
4. **Improve Debugging:** Facilitate quicker diagnosis of faults during design and production.

Key Techniques in DFT:

1. Scan-Based Testing:

- Converts flip-flops into scan cells to form a **scan chain**.
- Allows test vectors to be shifted into the design and observed during testing.
- Steps:
    1. **Shift Mode:** Load test patterns.
    2. **Capture Mode:** Apply functional logic and capture results.

2. Built-In Self-Test (BIST):

- Embeds testing circuits into the chip itself.
- Uses pattern generators and response analyzers to test functionality without external equipment.
- Common in memories (**Memory BIST**) and logic circuits (**Logic BIST**).

3. Boundary Scan (JTAG):

- Implements the IEEE 1149.1 standard for testing interconnects on printed circuit boards (PCBs).
- Adds a Test Access Port (TAP) and boundary scan cells to facilitate testing.

4. Logic Observability and Controllability:

- Improves the ability to control and observe internal signals during testing.
- Tools: Test Points (additional inputs or outputs for easier testing).

5. Fault Models:

- Simulate and detect specific faults:
    - **Stuck-At Faults:** Nodes stuck at 0 or 1.
    - **Delay Faults:** Timing errors.
    - **Transition Faults:** Issues with signal transitions.

Challenges in DFT:

1. **Area Overhead:**
    - Additional circuitry (e.g., scan chains, BIST logic) increases chip size.
2. **Performance Impact:**
    - DFT logic can introduce delays, impacting overall performance.
3. **Complexity:**
    - Integrating DFT techniques in complex designs requires careful planning and expertise.

Advantages of DFT:

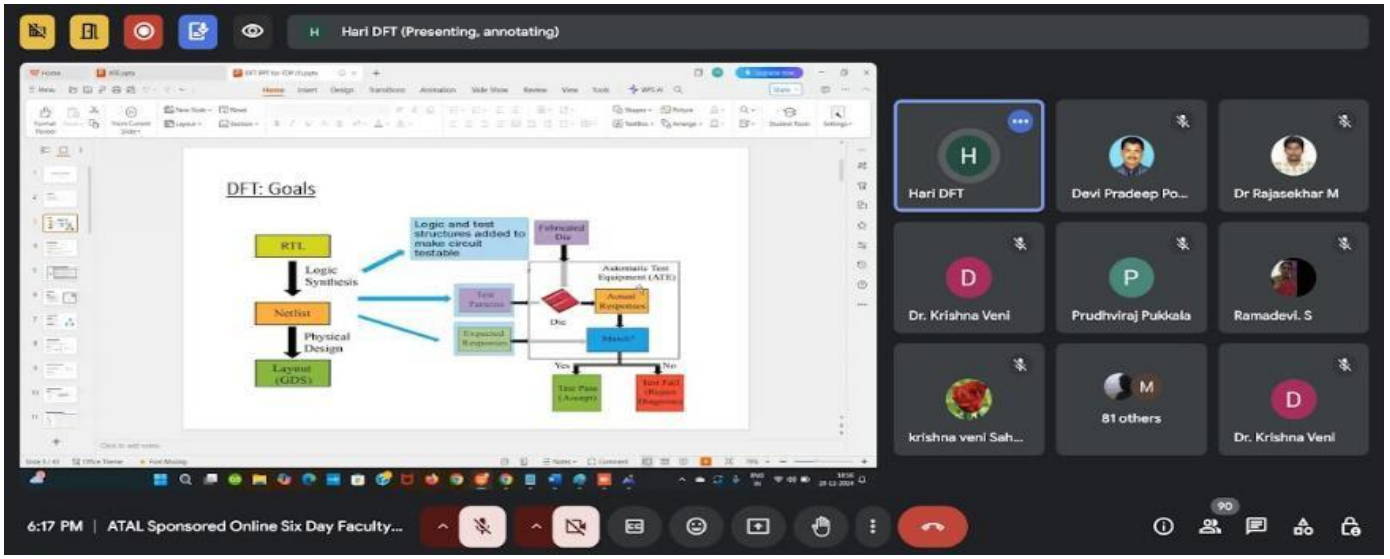
- **Higher Yield:** Detect and eliminate manufacturing defects early.
- **Reliability:** Ensures chips perform as intended in real-world applications.
- **Debugging Efficiency:** Speeds up fault diagnosis and repair during production.

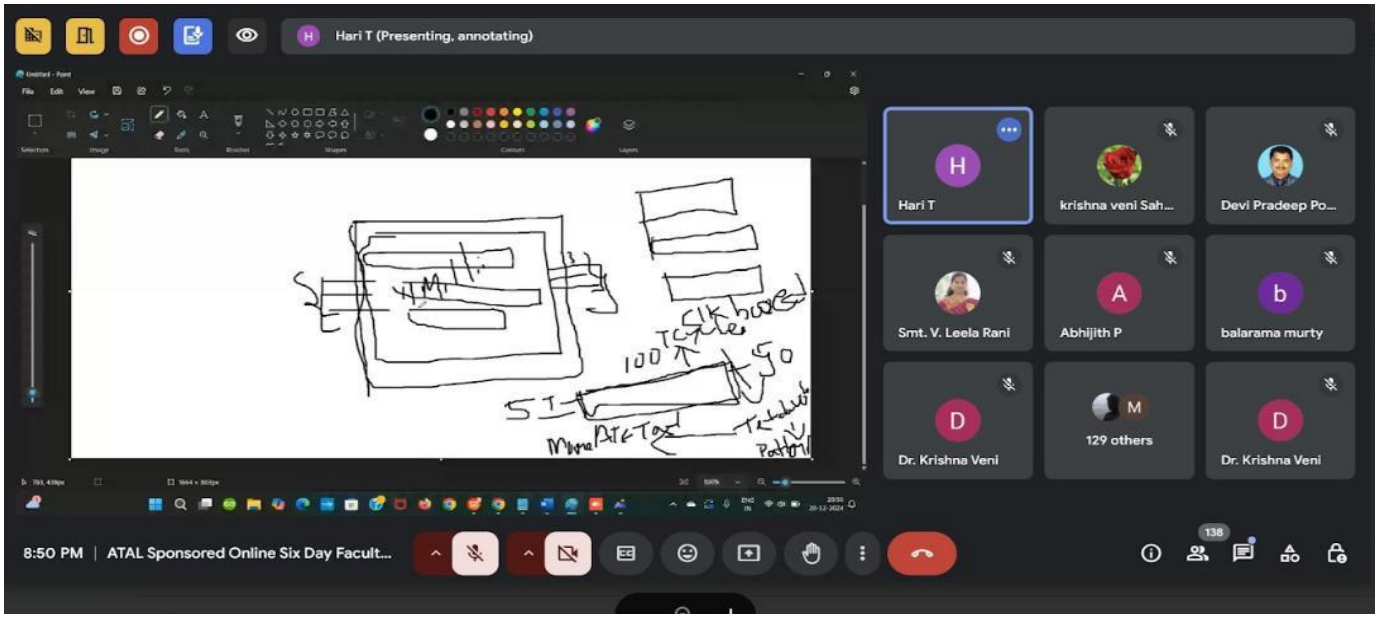
Importance of DFT in the VLSI Design Flow:

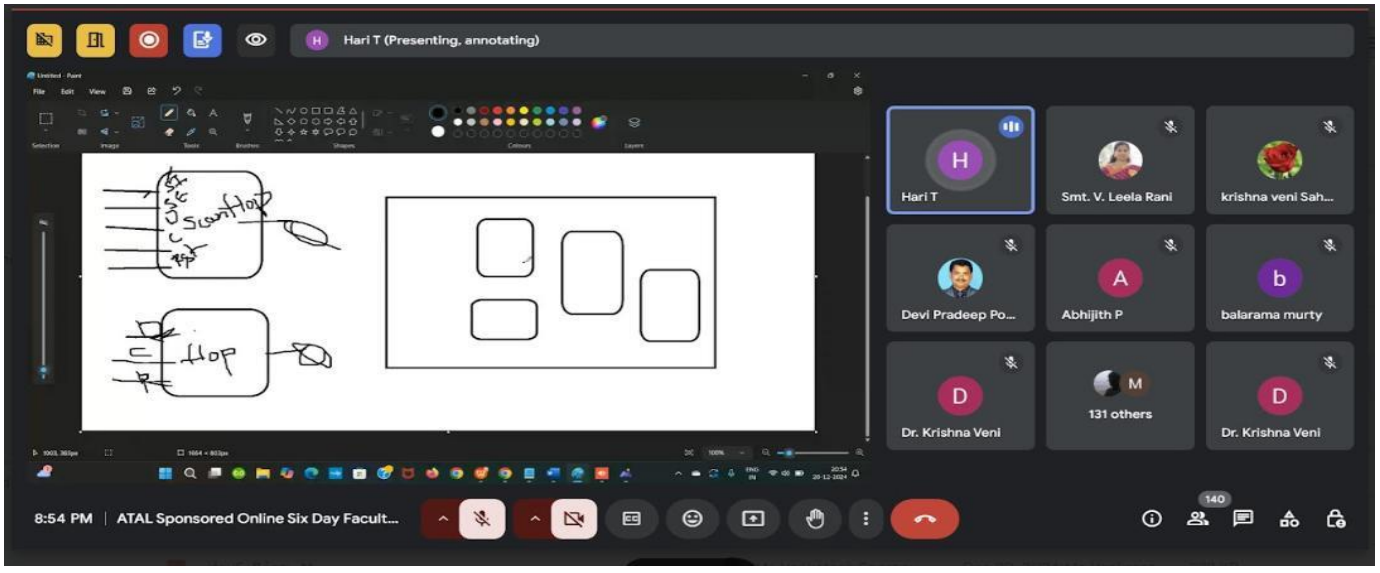
DFT is typically integrated during the design phase (pre-silicon) and verified post-silicon to ensure testability without compromising design goals like performance, area, or power.

Let me know if you'd like more details on any specific technique or tool!

Screen Shots of Day 5 Session 9 & Session 10:







Day 6 Session 11 & Session 12:

The **SOC protocol** (System on Chip protocol) refers to a set of rules and procedures that govern communication and interaction between different components of a System on Chip (SoC). An SoC integrates multiple components, such as processors, memory, input/output interfaces, and other hardware blocks, into a single chip. These protocols are essential for ensuring efficient data exchange, proper operation, and synchronization of the various parts of the SoC.

Some key aspects of SOC protocols include:

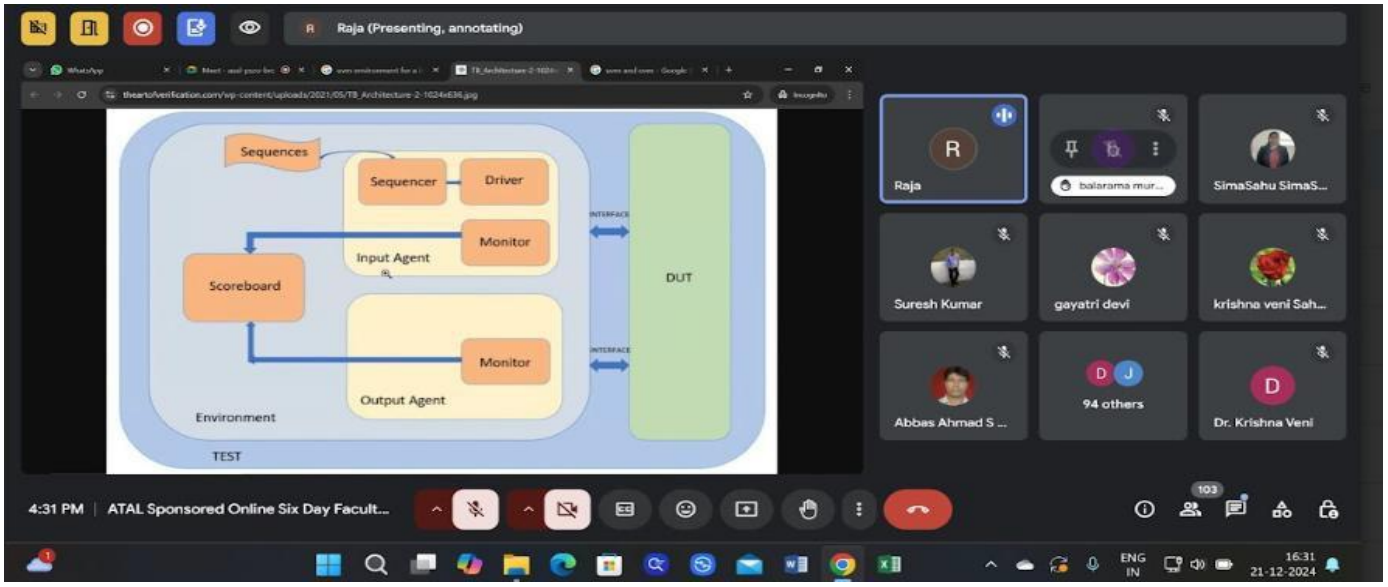
1. **Communication Protocols**: They define how data is transferred between different components of the SoC. Common communication protocols include:
   - **AMBA (Advanced Microcontroller Bus Architecture)**, used in ARM-based systems.
   - **AXI (Advanced eXtensible Interface)**, a high-performance interface for transferring data.
   - **APB (Advanced Peripheral Bus)**, a simpler bus for low-bandwidth peripherals.
   - **PCIe (Peripheral Component Interconnect Express)**, for high-speed communication between the chip and external components.
2. **Bus Protocols**: These protocols control how data is transmitted over the physical bus, ensuring that components can communicate without interference or data loss. Buses include **data**, **address**, and **control lines**.
3. **Power Management**: SOC protocols often include mechanisms for managing the power consumption of different parts of the system, switching components on and off based on activity.
4. **Security and Integrity**: Protocols in SoCs also include features for maintaining data integrity and security, especially in embedded systems that require secure data exchanges.
5. **Timing and Synchronization**: These protocols ensure that all components of the SoC work in sync, coordinating data flow without conflicts.

Digital Design involves creating circuits and systems using logic gates and hardware description languages (e.g., VHDL, Verilog). Key steps include specifying requirements, designing at the register-transfer level (RTL), synthesizing to gate-level, and optimizing for performance, power, and area.

Digital Verification ensures the design works as expected. It involves writing testbenches, simulating the design, using formal verification for critical properties, measuring coverage, and debugging. Tools like simulation and emulation platforms are used to detect and fix issues, ensuring the system meets specifications and timing constraints.

Together, these processes ensure that digital systems function correctly and efficiently.

Screen Shots of Day 6 Session 11 & Session 12:



Day 6 Session 13:

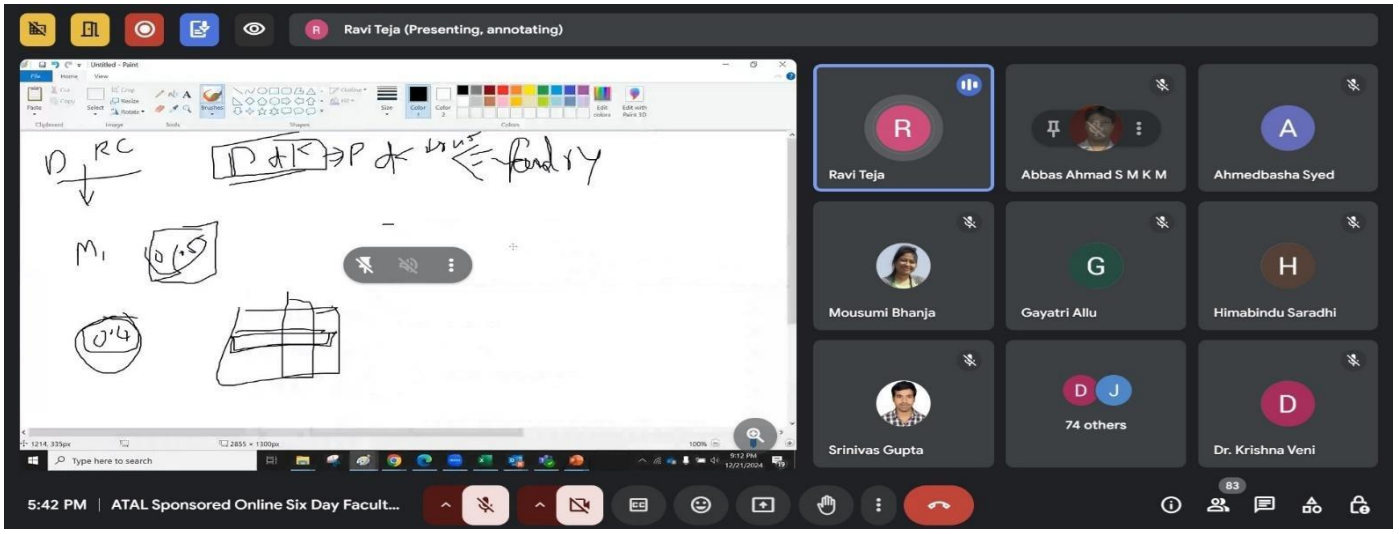
Custom layout design refers to the process of creating the physical layout of an integrated circuit (IC) at the transistor level, tailored to specific performance, power, and area requirements. It involves placing and routing the circuit components on the chip, ensuring that all connections are correct and meet timing and design constraints. Key aspects include:

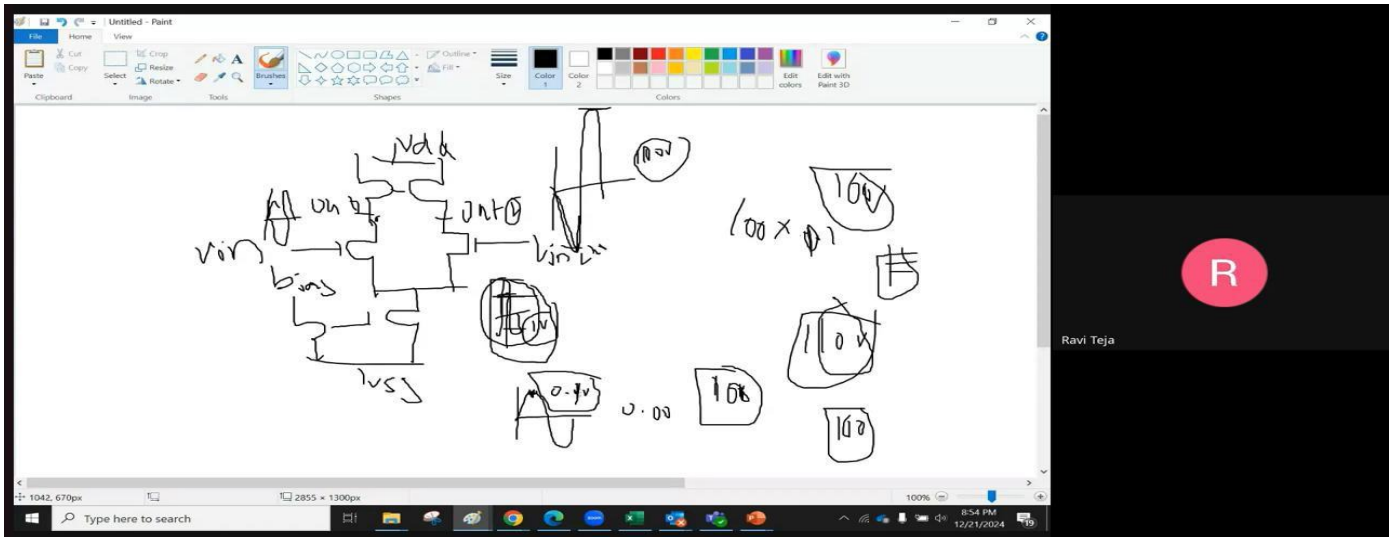
1. **Transistor Placement**: The precise positioning of transistors, resistors, and capacitors to optimize performance and minimize area.
2. **Routing**: Connecting components with metal layers while considering factors like signal integrity, power distribution, and minimizing delays.
3. **Design Rules**: Adhering to manufacturing rules (e.g., spacing, width) to ensure the layout can be fabricated without issues.
4. **Optimization**: Balancing trade-offs in power, performance, and area (PPA), often using advanced algorithms and techniques like floorplanning and clock-tree synthesis.
5. **Verification**: Ensuring the layout meets all design, electrical, and physical constraints, including DRC (Design Rule Check) and LVS (Layout vs. Schematic) checks.

Custom layout design is crucial for high-performance, low-power, or specialized ICs where standard cell libraries might not meet requirements.

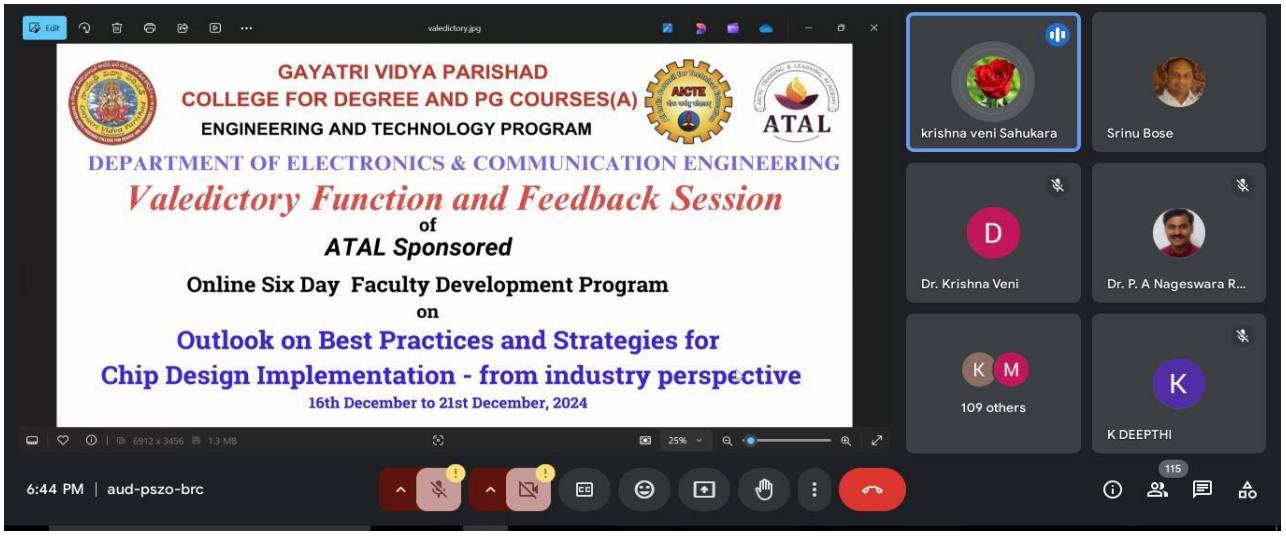
ATAL FDP on "OUTLOOK ON BEST PRACTICES AND STRATEGIES FOR CHIP DESIGN IMPLEMENTATION-FROM INDUSTRY PERSPECTIVE"

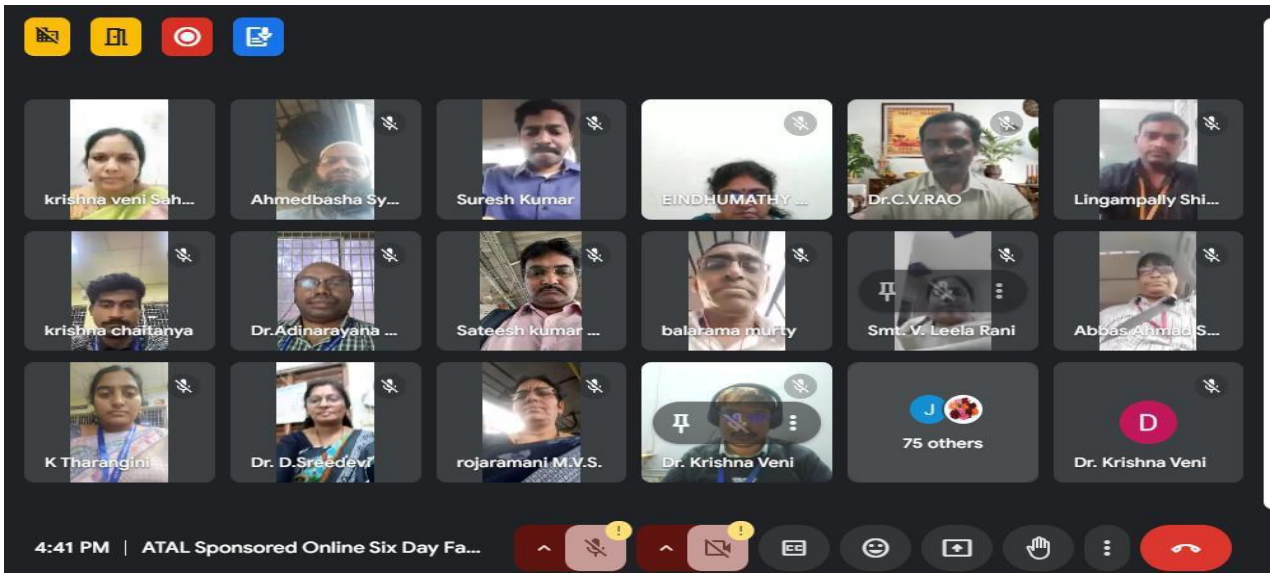
Screen Shots of Day 6 Session 13:

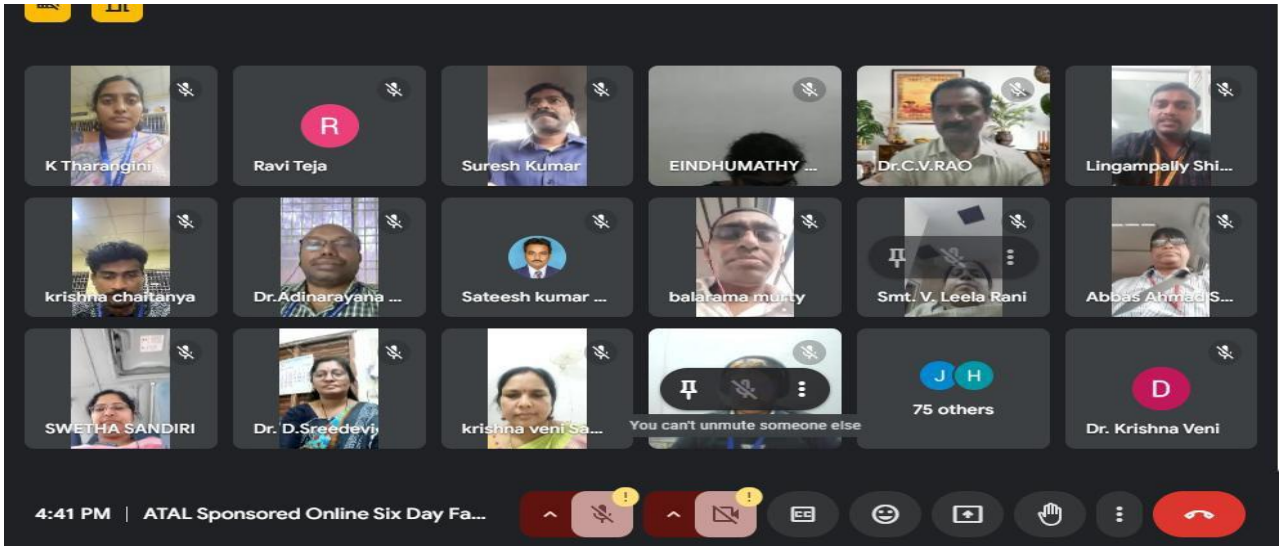




Valedictory Session:







Participants Feedback:

https://www.youtube.com/watch?v=f4B2cQMuvTM

00:06:36.849,00:06:39.849
Veerraju Sampenga: Thank you Madam for conducting this type of wonderful session

00:10:16.980,00:10:19.980
Aruna Kumari: Thank you so much mam for conducting this fdp gain more knowledge in practical domain applications

00:10:20.484,00:10:23.484
saisudheer kotta: All the sessions given by speakers were , very much information

00:10:37.359,00:10:40.359
Sridhar Done: Thank you Madam for conducting this type of wonderful session

00:10:50.570,00:10:53.570
prasannakumar mani: Thank you both the organizers

00:10:59.396,00:11:02.396
Akash Kumar Gupta: Thank you so much for conducting such informative session.

00:10:59.503,00:11:02.503
saisudheer kotta: And useful to academic and reserch

00:11:30.464,00:11:33.464
gowri thumbur: thank u organizers and speakers

00:12:05.626,00:12:08.626
Chukka Rajasekhar: Thanku very much Organizers

00:13:46.358,00:13:49.358
S MADHAVI: Thank you for a nice session

00:13:48.451,00:13:51.451
Neeraja Sajja: Thank very much organizers of this FDP. All the sessions are more informative.Expert speakers are given valuable lectures.

00:14:20.820,00:14:23.820
Sri Raju Paladugu: Thank you very much, FDP coordinators and speakers for providing VLSI opportunities in industry

00:14:34.507,00:14:37.507
K MAHESWARI: Thank you madam for conducting this type of wonderful and informative session

00:16:04.252,00:16:07.252
ADIL ZAIDI: Thanks to the organizers especially venkatesh sir for this special effort.

00:16:32.232,00:16:35.232
Mr. Tammineni Ravindra: Special Thanks to organizers

00:16:57.922,00:17:00.922
Sateesh kumar Gudla: Thank you very much, ATAL FDP coordinators and resource persons

00:18:18.862,00:18:21.862
P.BOSE BABU Assistant Professor: Thank you to Co-Ordinator's for giving an opportunity to attend the FDP. all the sessions are wonderful

00:23:56.835,00:23:59.835
Ramadevi. S: Thank you Coordinator and Organizers for conducting this FDP program

00:29:56.056,00:29:59.056
Surya Prasad: Very informative all sessions and Program organized well. Thank you GVP FDP coordinator and FDP Team

00:30:17.551,00:30:20.551
Dr Rajasekhar M: Thank you Dr. Krishna Veni Madam...

00:30:51.745,00:30:54.745
Rajesh Katragadda: Congratulations to DEPARTMENT of ECE for successfully conducting FDP

Press Clippings

మరింత నైపుణ్యత దిశగా శిక్షణ

సాగర్‌నగర్, న్యూస్‌టుడే: రుషికొండ గాయత్రీ విద్యాపరిషత్ (జీవీపీ) డిగ్రీ అండ్ పీజీ కోర్సుల కళాశాల ఈసీఈ విభాగం ఆధ్వర్యంలో సోమవారం నుంచి నిర్వహిస్తున్న ఆన్‌లైన్ జాతీయ స్థాయి ఫ్యాకల్టీ డెవలప్‌మెంట్ ప్రోగ్రాం (ఎఫ్‌డీపీ) శిక్షణను జీవీపీ ప్రిన్సిపల్ ఆచార్య కె.ఎస్.బోస్ ప్రారంభించారు. ఇస్రో పూర్వ శాస్త్రవేత్త డాక్టర్ రాధాకృష్ణన్ మాట్లాడుతూ పరిశ్రమలకు అనుగుణంగా విద్యావిధానం, బోధన రంగంలో మరింత నైపుణ్యత సాధించే దిశగా అధ్యాపకులు పాటించాల్సిన అంశాల్ని తెలియజేశారు. డైరెక్టర్ ఆచార్య పి.వి.వినయ్, డాక్టర్ పి.ఎ.నాగేశ్వరరావు, కన్వీనర్లు ఆచార్య ఎస్.కృష్ణవేణి, ఎస్.వెంకటేష్ మాట్లాడారు. ఆరు రోజుల పాటు ఆన్‌లైన్ విధానంలో జరిగే ఈ ఎఫ్‌డీపీ కార్యక్రమంలో దేశ వ్యాప్తంగా పలు విద్యాలయాలకు చెందిన చెందిన 200 మందికి పైగా బోధన సిబ్బంది పాల్గొన్నారన్నారు.

■ ముగిసిన బోధన సిబ్బంది శిక్షణ

సాగర్‌నగర్, న్యూస్‌టుడే: రుషికొండ గాయత్రీ విద్యాపరిషత్ (జీవీపీ) డిగ్రీ అండ్ పీజీ కోర్సుల కళాశాల ఈసీఈ విభాగం ఆధ్వర్యంలో నిర్వహించిన ఆన్‌లైన్ జాతీయస్థాయి ఫ్యాకల్టీ డెవలప్‌మెంట్ ప్రోగ్రామ్ శిక్షణ శనివారంతో ముగిసింది. పరిశ్రమలకు అనుగుణంగా విద్యావిధానం, బోధన రంగంలో మరింత నైపుణ్యత సాధించే దిశగా అధ్యాపకులు అనుసరించాల్సిన వ్యూహాలు, నూతన ఆవిష్కరణల అంశాలను శిక్షణలో చర్చించారు.

फैकल्टी डेवलपमेंट प्रोग्राम (एफडीपी) का समापन समारोह...

admin December 22, 2024 प्रादेशिक
Leave a comment 10 Views

Jdñews Vision...

एआईसीटीई ट्रेनिंग एंड लर्निंग (एटीएएल) अकादमी द्वारा प्रायोजित फैकल्टी डेवलपमेंट प्रोग्राम (एफडीपी) का समापन समारोह "चिप डिजाइन कार्यान्वयन के लिए सर्वोत्तम प्रथाओं और रणनीतियों पर दृष्टिकोण" पर गायत्री विद्या परिषद कॉलेज के डिग्री और पीजी पाठ्यक्रमों के लिए ईसीई विभाग में सफलतापूर्वक आयोजित किया गया। आचार्या एस. कृष्ण वेणी द्वारा संचालित इस छह दिवसीय कार्यक्रम में देश भर के विभिन्न प्रतिष्ठित संगठनों के 185 प्रतिनिधियों ने भाग लिया।
शिक्षा जगत और उद्योग जगत के जाने-माने संसाधन व्यक्ति इस क्षेत्र में सर्वोत्तम प्रथाओं, उभरती रणनीतियों और अत्याधुनिक नवाचारों पर ध्यान केंद्रित करेंगे। विचारोत्तेजक सत्र और आकर्षक व्याख्यान दिए गए। इस कार्यक्रम में प्राचार्य आचार्य. के.एस. बोस, निदेशक प्रो. पी.वी. विनय, ई.सी.ई. विभागाध्यक्ष डॉ. पी.ए. नागेश्वर राव, समन्वयक आचार्या एस. कृष्ण वेणी, एस. वेंकटेश और अन्य ने भाग लिया।

It was a great Initiative by ATAL Academy. I am thankful to AICTE for giving me this opportunity to conduct online FDP for faculty members of technical institutions of India for free of cost. I got huge response for registration as well as lots of compliment of arranging the online FDP'S, content relevant to bridge the gap between industry and academia as well as research perspective.

GAYATRI VIDYA PARISHAD
COLLEGE FOR DEGREE AND PG COURSES (A)
ENGINEERING AND TECHNOLOGY PROGRAM
DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING
A 5 DAYS PROGRAM ON UNMANNED AERIAL SYSTEMS

Details of the Program

Title of the Program	:	Unmanned Aerial Systems
Number of days	:	05
Training Agency involved	:	National institute of Electronics and Information technology, Aurangabad
Name of the Trainer's	:	Mr.Rhisi Das And Mr. Vaibav, Assistant Professors, Department of Electronics and Communication Engineering, NIELIT, Aurangabad
Objective of the program	:	➢ To provide participants with a comprehensive understanding of the specific emerging technology ➢ To enable participants to develop practical skills through hands-on learning activities. ➢ To foster a collaborative learning environment where participants can engage with instructors and peers. ➢ To empower participants to apply their knowledge to real-world scenarios and projects. ➢ To empower participants to identify opportunities for implementation of skills within their organizations, self-driven activities etc.
Outcome of the program	:	1. Introduction of Drone UAV, types of drones, subsystems of drones. 2. Basic aerodynamics: How drones fly and maintain stability in the air. 3. Understand the function of each major drone component. 4. Introduction and familiarization of various communication Protocols. 5. Acquire the ability to troubleshoot and replace faulty components. 6. Knowing different type of sensors in UAV. 7. Learn how to assemble, disassemble, and maintain drone parts. 8. Hands on practicals on Drone UAV and Mission Planning Software. 9. Calibration of Drone and Flight Modes. 10. Autonomous Flight Systems 11. Flight algorithms, sensor integration, and control systems 12. Raspberry pi and Jetson nano. 13. Communication with Raspberry pi.
Number of Students Registered	:	104 (IV year – 24, III year – 46, II year – 34)
Name of the faculty organiser	:	Mrs. A. Aruna, Assistant Professor, Mrs. K. Deepthi, Assistant Professor, Department of Electronics and Communications Engineering, GVPCDPGC(A)

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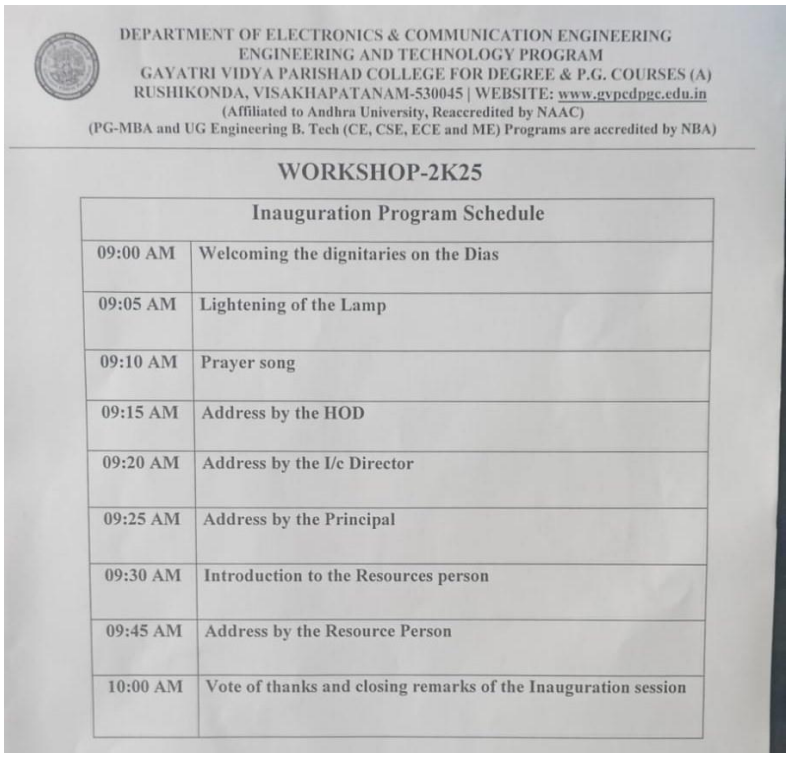
COLLEGE FOR DEGREE AND PG COURSES (A)
ENGINEERING AND TECHNOLOGY PROGRAM
DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING
A 5 DAYS PROGRAM ON UNMANNED AERIAL SYSTEMS

Detailed Report

Day 1 – 06.01.2025 (Forenoon)

Introduction

The inauguration ceremony for the Unmanned Aerial Systems Program was held with enthusiasm and participation from diverse stakeholders, including participants, instructors, and distinguished guests. The event aimed to set the tone for an enriching program that combines emerging technology insights with hands-on learning experiences.



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RUSHIKONDA, VISAKHAPATANAM-530045 | WEBSITE: www.gvpcdpgc.edu.in
(Affiliated to Andhra University, Reaccredited by NAAC)
(PG-MBA and UG Engineering B. Tech (CE, CSE, ECE and ME) Programs are accredited by NBA)

WORKSHOP-2K25

Inauguration Program Schedule	
09:00 AM	Welcoming the dignitaries on the Dias
09:05 AM	Lightening of the Lamp
09:10 AM	Prayer song
09:15 AM	Address by the HOD
09:20 AM	Address by the I/c Director
09:25 AM	Address by the Principal
09:30 AM	Introduction to the Resources person
09:45 AM	Address by the Resource Person
10:00 AM	Vote of thanks and closing remarks of the Inauguration session

Schedule of the program

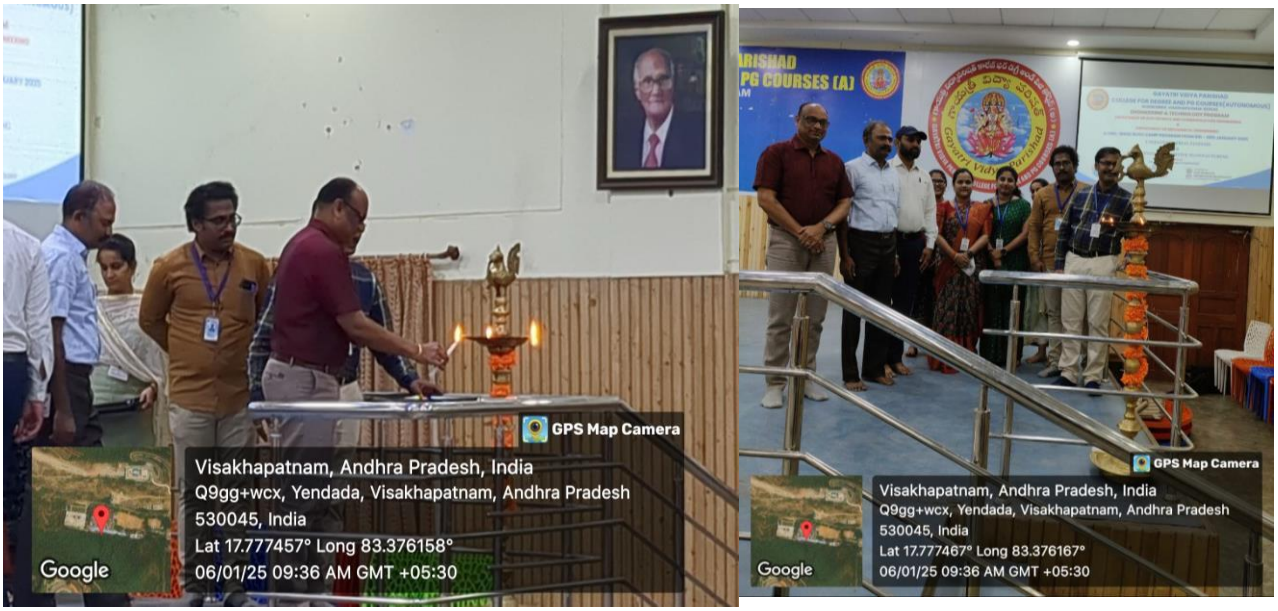
Welcome and Opening Remarks

The ceremony began with a warm welcome address by Dr.CH.Hima Gireesh & Dr.P.A.Nageswara Rao, HOD, Department of Mechanical & Department of ECE, who highlighted the importance of integrating CAD design and 3D printing and Drone Technologies in today's technological landscape. They emphasized how the program aligns with the objectives of empowering participants with practical skills and fostering innovation in real-world applications.

Keynote Address

The keynote speech was delivered by Mr Zulfiker Ali, Assistant Professor, Department of Mechanical Engineering, NIELIT, Aurangabad, a notable expert in the field of 3D printing and CAD design. Their address provided insights into the growing significance of additive manufacturing and its applications

across various industries. They also encouraged participants to embrace the opportunities offered by this cutting-edge technology.



Prof.K.S.Bose, Principal, GVPCDPC(A), Lightening the lamp

Prof.K.S.Bose, Principal, GVPCDPC(A) addressing the participants

Closing Remarks

The ceremony concluded with a vote of thanks delivered by Smt. K. Aruna, Assistant Professor, Department of ECE, expressing gratitude to the Speakers, participants, and guests. The speaker reiterated the program's mission to empower participants to apply their knowledge effectively in their respective fields.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING
A 5 DAYS PROGRAM ON UNMANNED AERIAL SYSTEMS

Day 1 – 06.01.2025

The topics which are to be delivered by the resource person are listed below:

Day 1: Monday, January 06, 2025	
10:00-11:30	Introduction of Drone UAV.
11:30-11:45	TEA BREAK
11:45-13:00	Types of drones: Fixed-wing vs. multirotor drones (quadcopters, hexacopters, octocopters).
13:00-14:00	LUNCH BREAK
14:00-15:30	Subsystems of drone.
15:30-15:45	TEA BREAK
15:45-17:00	Basic aerodynamics: How drones fly and maintain stability in the air.

Therefore, as per the designed syllabus

Module 1: Introduction to Unmanned Aerial Systems (UAS) - Report

The first module of the UAS Training Program, titled **Introduction to Unmanned Aerial Systems (UAS)**, was an informative and engaging session that provided participants with a thorough understanding of UAVs and their core components. The module began with a detailed introduction to **Unmanned Aerial Vehicles (UAVs)**, commonly known as drones, explaining their role in modern technology and their diverse applications across industries such as agriculture, surveillance, defense, and delivery systems.

Types of drones:

The instructors explained the basic concept of UAVs as remotely controlled or autonomously flying aircraft systems. Participants were introduced to the different **types of wings** used in UAV design, including **fixed wings**, **rotary wings**, and **hybrid designs**, along with their respective uses. The distinctions between **fixed-wing UAVs** for long-range flights and **rotary-wing UAVs** for more agile, vertical take-off and landing (VTOL) capabilities were clarified.

Mr.Rishi Das explaining the students about the topic on unmanned aerial systems

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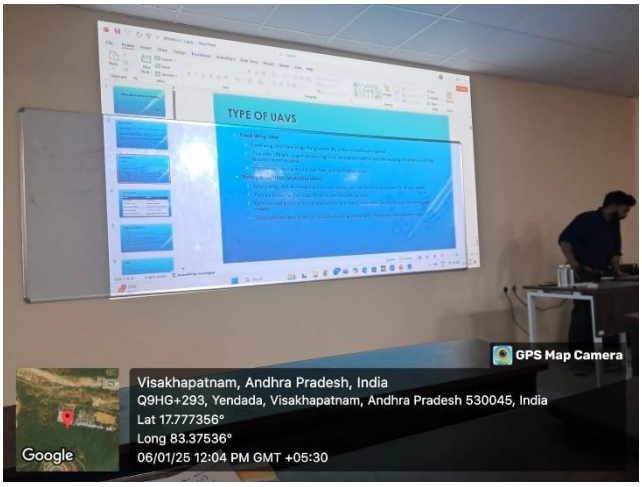
The session also provided insights into the **classification of UAVs based on their sizes**, from small **nano UAVs** to larger **strategic UAVs** used for military applications. Furthermore, participants learned about **rotor-based UAVs**, with categories like **quadcopters**, **hexacopters**, and **octocopters**, each designed to offer specific advantages in flight stability and payload capacity.

Subsystems of drone :

The instructors emphasized the importance of understanding UAV **subsystems**—such as the **power system**, **propulsion system**, **flight control system**, **navigation**, and **payload**—in building efficient and functional UAVs. The role of **communication systems** in ensuring remote control and data transfer was also discussed in detail.

Participants were then introduced to the **airspace zones** where UAVs are permitted to operate, including **controlled** and **uncontrolled airspace**, **no-fly zones**, and **temporary flight restrictions (TFRs)**. The importance of complying with airspace regulations was emphasized to ensure safety and efficiency in UAV operations.



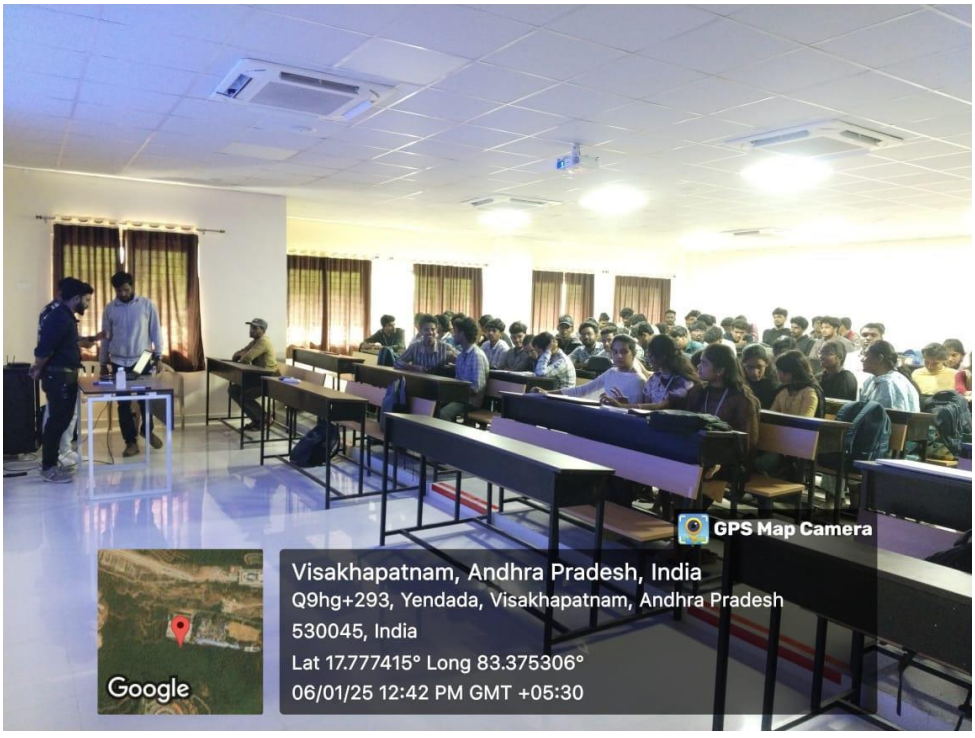
Mr.Rhisi Das, Trainer, Assistant professor, NIELIT discussing with students related to subsystems of drone

An important part of the session focused on the **forces involved in drone flight**, explaining the four key forces: **lift**, **thrust**, **drag**, and **weight**, and their impact on drone performance. The mentors clarified the essential principles of flight dynamics and how they relate to the design and control of UAVs.

Additionally, an in-depth explanation of UAV **wing structures (aerofoils)** was provided, helping participants understand how the shape of wings affects lift generation and stability. This led to discussions on the principles of Throttle **throttle, pitch**, **roll**, and **yaw**, which are the primary motions that control a drone's orientation and direction during flight.

The module concluded with a discussion on the **protocols for creating drones**, focusing on the design, testing, assembly, and regulatory compliance processes involved in building an efficient and reliable UAV. The mentors outlined the various **approaches for drone-making**, including selecting materials, conducting simulations, and ensuring safe operation.

Interactive discussions and Q&A sessions encouraged participants to ask questions and clarify any doubts, fostering a collaborative learning environment. The session concluded with a summary of key takeaways and an overview of the upcoming topics in the program.



Mr.Rhisi Das, NIELIT discussing with students related to the topic

Overall, **Module 1** provided participants with a solid foundation in the principles, components, and regulations of UAV technology, setting the stage for more advanced topics in the field.

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Detailed Report

Day 2 – 07.01.2025 (Forenoon)

The topics which are to be delivered by the resource person are listed below:

Day 2: Tuesday, January 07, 2025	
10:00-11:30	Understand the function of each major drone component
11:30-11:45	TEA BREAK
11:45-13:00	Introduction and familiarization of various communication Protocols.
13:00-14:00	LUNCH BREAK
14:00-15:30	Acquire the ability to troubleshoot and replace faulty components
15:30-15:45	TEA BREAK
15:45-17:00	Different type of sensors in UAV.

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Module 2: Components of Unmanned Aerial Systems (UAS) - Report

The second module of the UAS Training Program, titled **Components of Unmanned Aerial Systems (UAS)**, was a comprehensive session aimed at introducing participants to the essential hardware components that power and control a drone. This module was critical for providing the foundational knowledge required to understand how each part of the drone contributes to its flight, performance, and capabilities.

The session began with an engaging overview of **key drone components**, starting with **propellers** and moving into more complex systems such as **motors**, **flight controllers**, and **sensors**. The instructors emphasized the importance of understanding each component's role in ensuring the drone functions properly and can perform specific tasks, such as stable flight, navigation, and obstacle avoidance.

Instructors explaining the components of drones

The instructors provided detailed explanations on the **Brushless DC Motors (BLDC)**, **Electronic Speed Controllers (ESC)**, and how these systems work in tandem to control the drone's speed and movement. Participants were introduced to the role of the **flight controller** as the brain of the drone, handling commands and processing data from various sensors to maintain stability during flight.

Mr.Rishi Das, Trainer, Assistant professor, NIELIT discussing with students related to drone components

The module also delved into more advanced hardware, such as the **Arduino** and **Raspberry Pi**, which are used for programming and controlling various drone functions. The instructors highlighted the importance of **ARM controllers** and how these microcontrollers enable real-time flight control by processing sensor data efficiently.

Day 2 – 07.01.2025 (Afternoon)

Instructors explaining sensors and telemetry systems

The instructors provided an in-depth explanation of **sensors** and their crucial role in the operation of drones. A **sensor** is a device that collects data from the drone's environment and transmits this information to the **flight controller** for processing and control. This real-time data collection allows the drone to adjust its flight path and behaviour, ensuring stability, navigation, and responsiveness to environmental changes.

The data captured by sensors can include key parameters such as **altitude**, **position**, **speed**, and **orientation**. Additionally, sensors can measure external environmental factors like **temperature** and **humidity**, which may affect drone performance. The importance of sensors in providing accurate, timely feedback to the flight controller was emphasized, as it enables safe and efficient drone operations.

Mr.Zulfiker Ali, Trainer, Assistant professor, NIELIT discussing with students related to the topic

Moving to the battery systems, the session highlighted the different types of **batteries** used in drones, especially **Lithium-Polymer (LiPo)** batteries, known for their high energy density and efficiency. The instructors discussed how the right battery selection impacts the drone's performance, particularly in terms of flight time and payload capacity.

The instructors also explained the **remote controller/transmitter** systems used to communicate with the drone and control its flight. **Telemetry** systems, which provide real-time flight data to the operator, were discussed in detail, emphasizing their importance for maintaining safe and efficient drone operations.

Instructors discussing the role of telemetry and protocols in drone systems

The final part of the module focused on **communication protocols** and **firmware**. The instructors elaborated on the importance of protocols like **PWM**, **I2C**, **UART**, and **MAVLink**, which facilitate smooth communication between the various components of the drone. The discussion on **firmware** covered how this embedded software allows the hardware to function properly, with frequent updates required to optimize performance and incorporate new features.

Interactive Q&A segments allowed participants to share their insights and clarify any doubts, fostering a collaborative learning environment.

Mr.Rishi Das, Trainer, Assistant professor, NIELIT discussing with students related role of telemetry and protocols in drone systems

The module concluded with a summary of key takeaways and a preview of upcoming topics in the program. Overall, **Module 2** provided participants with a thorough understanding of the essential components that make up a drone, setting the stage for more advanced discussions on drone systems and operations.

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Detailed Report

Day 3 – 08.01.2025 (Forenoon)

The topics which are to be delivered by the resource person are listed below:

Day3: Wednesday, January 08, 2025	
10:00-11:30	Learn how to assemble, disassemble, and maintain drone parts.
11:30-11:45	TEA BREAK
11:45-13:00	Learn how to assemble, disassemble, and maintain drone parts.
13:00-14:00	LUNCH BREAK
14:00-15:30	Hands on practicals on Drone UAV and Mission Planning Software.
15:30-15:45	TEA BREAK
15:45-17:00	Calibration of Drone and Flight Modes.

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Module 3: Assembling of Drone Components - Report

The third module of the Unmanned Aerial System (UAS) Training Program, titled **Assembling of Drone Components**, was an essential session designed to provide participants with practical knowledge and skills in assembling and aligning key drone components. The module commenced with an engaging overview of the importance of proper component alignment for ensuring optimal drone performance and stability.

Mr.Rishi Das, Trainer, explaining how to assemble drone parts

The instructors emphasized the critical aspects of drone assembly, explaining the role of each component and its effect on the drone's overall functioning. Participants were introduced to the key drone components such as the battery holder, landing gear (lander stand), arms, and Electronic Speed Controllers (ESCs), with a special focus on the importance of aligning and soldering these parts correctly for safe and efficient flight

Key Topics Covered:

- **Battery Holder Alignment**: The instructor began by explaining how the battery holder plays a crucial role in securing the drone's power source. Emphasis was placed on proper alignment to ensure balanced weight distribution, which is essential for stable flight. Techniques for securely mounting the battery to avoid shifting during flight were discussed in detail.

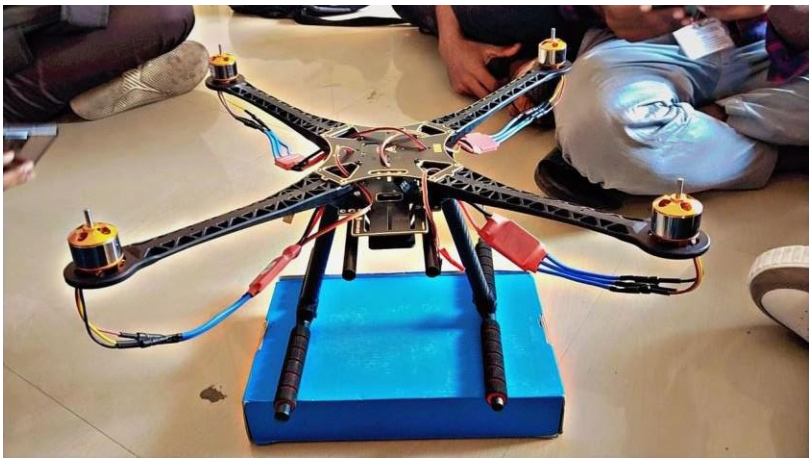
- **Landing Gear (Lander Stand) Setup**: The session continued with an in-depth explanation of the landing gear's importance in protecting the drone during takeoff and landing. The instructor demonstrated how to properly align the landing gear to absorb impact and provide stability, ensuring that the drone can land safely without damage.
- **Arm Placement and Symmetry**: The arms, which hold the motors and propellers, are crucial for the drone's flight performance. The instructor demonstrated how to correctly align the arms, ensuring that the drone maintains a symmetrical structure to facilitate balanced and controlled flight. Misalignment of the arms was discussed as a key cause of flight instability.

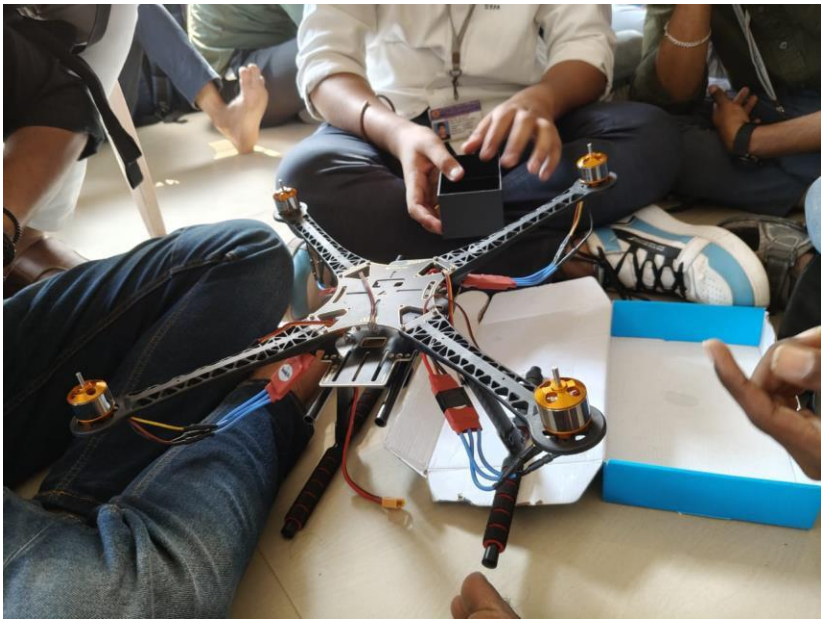
- **ESC Connections and Soldering**: The module also covered the process of soldering the ESCs to the motors, which control the speed of the motors. The instructor explained the importance of secure, accurate soldering connections to ensure smooth power distribution. Practical soldering techniques were demonstrated, and students had the opportunity to practice these skills under supervision.

Practical Demonstrations:

The module incorporated practical, hands-on sessions, allowing students to align and install the drone components themselves. Under the guidance of the instructor, participants practiced soldering ESC connections and aligning the battery holder, arms, and landing gear. This hands-on experience helped students develop the technical skills necessary for assembling drones effectively and safely.

Mr.Rishi Das, the instructor for the session, guided participants through each process, providing valuable insights into the technicalities of drone assembly and troubleshooting common issues. Interactive Q&A sessions allowed students to clarify any doubts, fostering a collaborative learning atmosphere.





Students assembling the parts of drone

Module 3 was a highly engaging and informative session, successfully providing participants with foundational knowledge and skills in drone component alignment and assembly. The balance between theory and hands-on practice ensured that participants left the session with a solid understanding of drone setup and the necessary skills for building functional UAS.

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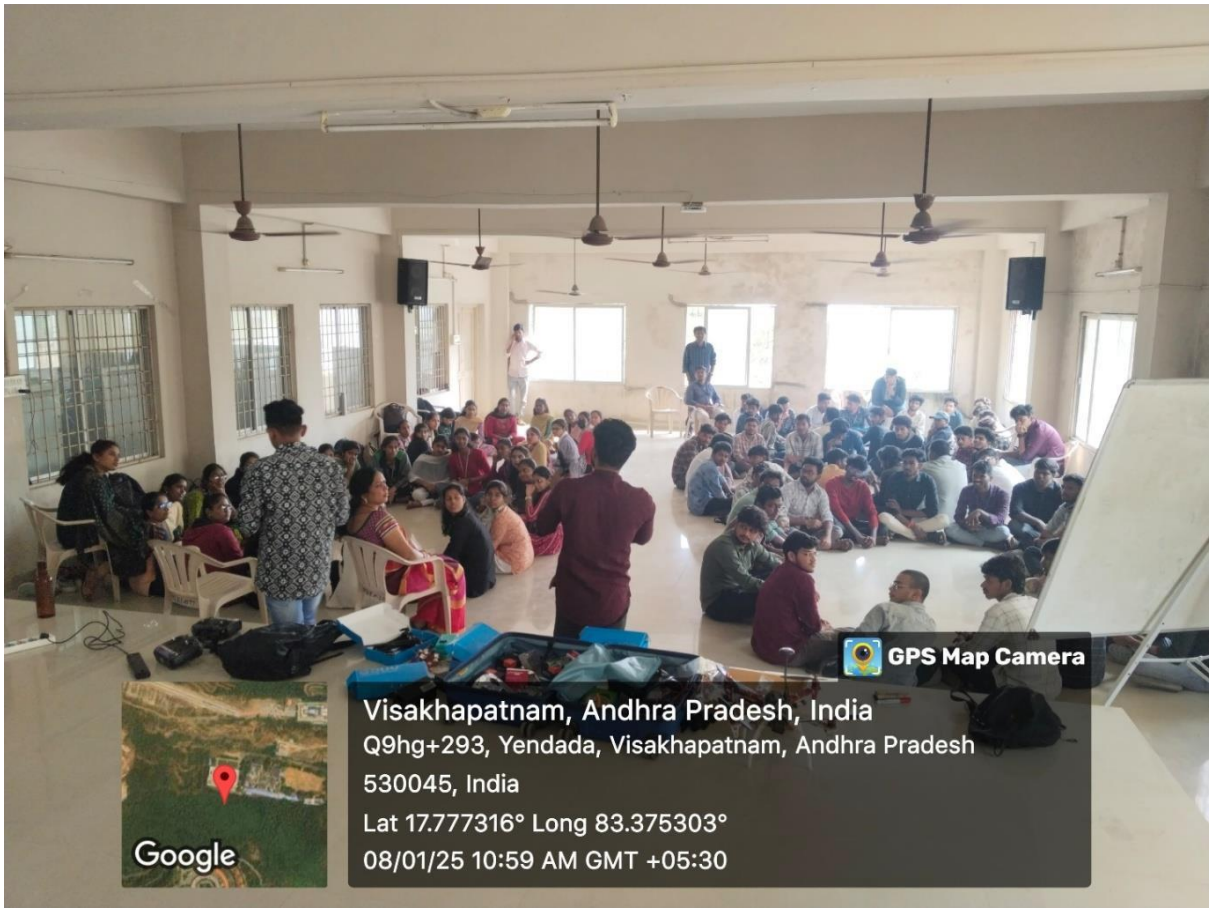
Looking Ahead:

- Continued practice in assembling drone components and refining soldering skills.
- Introduction to the integration of drone systems and the fundamentals of power distribution.
- Preparation for the upcoming flight testing and calibration phase.



Mr.Rishi Das, Trainer, Assistant professor, NIELIT discussing with students related to disassemble the drone parts.

Module 3 successfully equipped participants with essential knowledge and hands-on experience in aligning and assembling drone components. This foundational session has paved the way for participants to confidently dive into more advanced topics, including system integration, flight testing, and optimization in the following modules.

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Detailed Report

Day 4 – 09.01.2025 (Forenoon)

The topics which are to be delivered by the resource person are listed below:

Day 4: Thursday, January 09, 2025	
10:00-11:30	Autonomous Flight Systems
11:30-11:45	TEA BREAK
11:45-13:00	Flight algorithms, sensor integration, and control systems
13:00-14:00	LUNCH BREAK
14:00-15:30	Raspberry pi and Jetson nano.
15:30-15:45	TEA BREAK
15:45-17:00	Communication with Raspberry pi.

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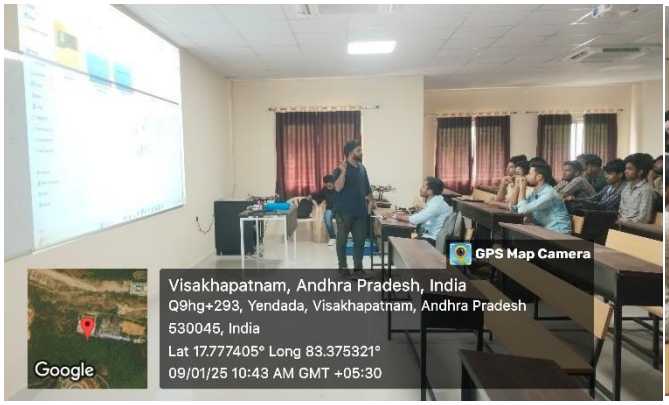
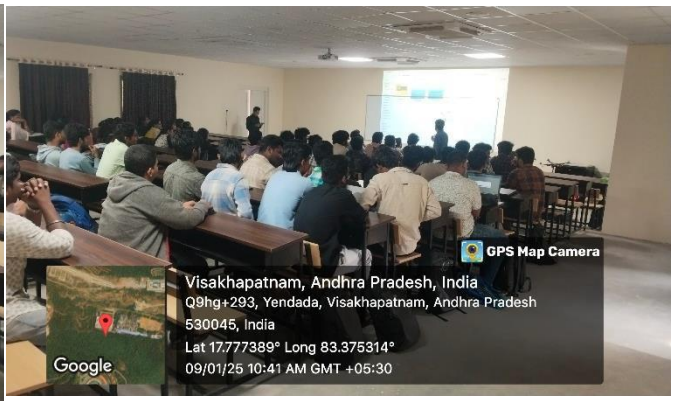
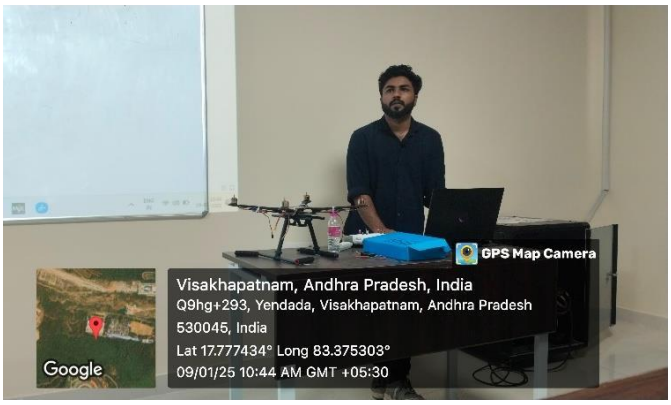
Module 4: Advanced Operations and Simulation of Unmanned Aerial Systems (UAS) - Report

The fourth module of the Unmanned Aerial Systems Training Program, titled **Advanced Operations and Simulation of Unmanned Aerial Systems (UAS***)*, was a comprehensive session that focused on integrating drone hardware with software and simulation tools. This module laid the groundwork for advanced drone operations, emphasizing both theoretical concepts and practical applications.





The session began with a continuation of the previous day's topics, diving deeper into the connection and configuration of key components such as the ESC (Electronic Speed Controller) and flight controller. Participants were guided step-by-step through the process of connecting the ESC and the receiver to the flight controller, with an in-depth explanation of the pins and their respective roles.



The instructors introduced participants to **Mission Planner**, a software tool used for configuring, calibrating, and simulating drone operations. They explained the following calibration procedures: accelerometer calibration, compass sensor calibration, remote controller synchronization, and ESC setup for motor control. Additionally, flight modes and fail-safe configurations were discussed, highlighting their importance in ensuring safe and efficient drone operations.

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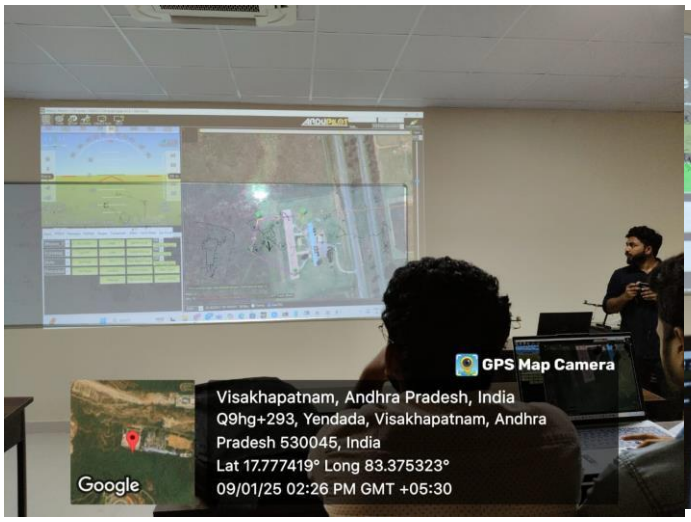
Day 4 – 09.01.2025 (Afternoon)

Instructors explaining about the components and configurations of drones

In the afternoon session, participants were introduced to the procedure for simulating drone operations using Mission Planner. The step-by-step demonstration included selecting a quadcopter model, downloading the required plane files, setting locations, adjusting parameters, and initiating simulation through mission actions. This hands-on exercise enabled participants to gain a practical understanding of simulating and testing drone operations in a controlled environment.



Mr.Rishi Das, Trainer, Assistant professor, NIELIT discussing with students related to the Mission Planner software

The session also delved into the integration of Raspberry Pi with drones. The instructor explained the connection of the Raspberry Pi to a laptop and its significance in programming drone functionalities. Participants were introduced to essential terminal commands such as cd, ls, mkdir, and nano, which are used to navigate and manage files in a Linux-based system. Basic programming in the C language was also demonstrated using the terminal, emphasizing its importance in developing and controlling drone applications.

Interactive Q&A segments throughout the session encouraged participants to ask questions and clarify doubts, creating a collaborative learning environment.

Mr.Zulfiker Ali, Trainer, Assistant professor, NIELIT discussing with students related to the topic

The module concluded with a summary of key takeaways and a preview of the upcoming topics in the program. Overall, Module 4 provided participants with a solid foundation in advanced drone operations, including hardware configuration, simulation, and programming, setting the stage for more sophisticated applications in unmanned aerial systems.

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Detailed Report

Day 5 – 10.01.2025 (Forenoon)

The topics which are to be delivered by the resource person are listed below:

Day 5: Friday, January 10, 2025	
10:00-11:30	Flight algorithms, sensor integration, and control systems
11:30-11:45	TEA BREAK
11:45-13:00	MCQ Based Test
13:00-14:00	LUNCH BREAK
14:00-15:30	Drone Fly
15:30-15:45	TEA BREAK
15:45-17:00	Certificate Distribution

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Day 5: Final Day of the Unmanned Aerial Systems (UAS) Boot Camp – Report

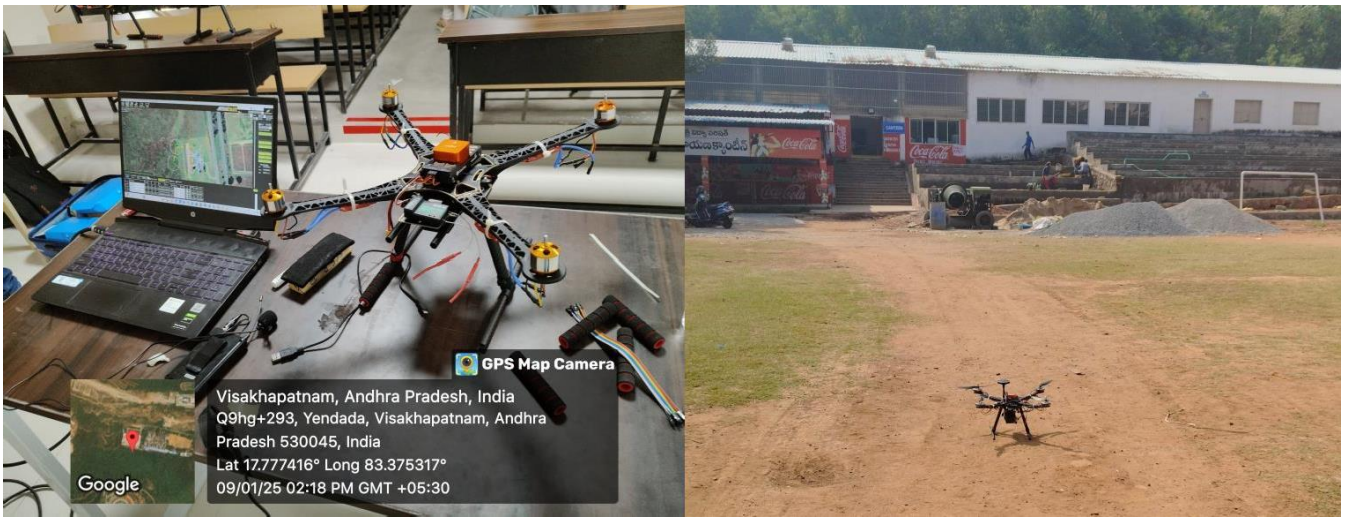
The final day of the **Unmanned Aerial Systems (UAS) Boot Camp**, held on **10th January 2025**, was a blend of evaluation, live demonstrations, and celebration, marking the conclusion of an enriching week-long program

Morning Session: Online Examination

The day commenced with an online exam designed to evaluate participants' grasp of the concepts and skills acquired during the boot camp. The exam tested topics such as drone assembly, flight principles, and programming, providing an opportunity for participants to showcase their learning.The instructors introduced participants to *Mission Planner*, a software tool used for configuring, calibrating, and simulating drone operations. They explained the following calibration procedures: accelerometer calibration, compass sensor calibration, remote controller synchronization, and ESC setup for motor control. Additionally, flight modes and fail-safe configurations were discussed, highlighting their importance in ensuring safe and efficient drone operations.

Drone Ground Testing

Following the examination, the instructors conducted live drone testing in the ground area of GVP. The drones assembled by participants during the boot camp were evaluated for functionality, stability, and flight readiness. This practical demonstration allowed participants to witness the culmination of their efforts, reinforcing their understanding of drone operations and troubleshooting.



Mr.Rishi Das, Trainer, Assistant professor, NIELIT conducted live drone testing in the ground of GVP

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Day 5 – 10.01.2025 (Afternoon)

Afternoon Session: Valedictory Ceremony

The afternoon session was dedicated to the valedictory ceremony, marking the successful conclusion of the boot camp. Several participants shared heartfelt reflections on their experiences, expressing gratitude for the hands-on learning opportunities, collaborative teamwork, and the invaluable mentorship provided throughout the program. Certificates of completion were distributed to all participants by the Dean of the college, along with the Heads of the Departments of Electronics and Communication Engineering and Mechanical Engineering. As a gesture of appreciation, mementos were presented to the instructors, Mr. Rishi Das and Mr. Vaibhav, whose expertise and guidance played a pivotal role in the program's success.

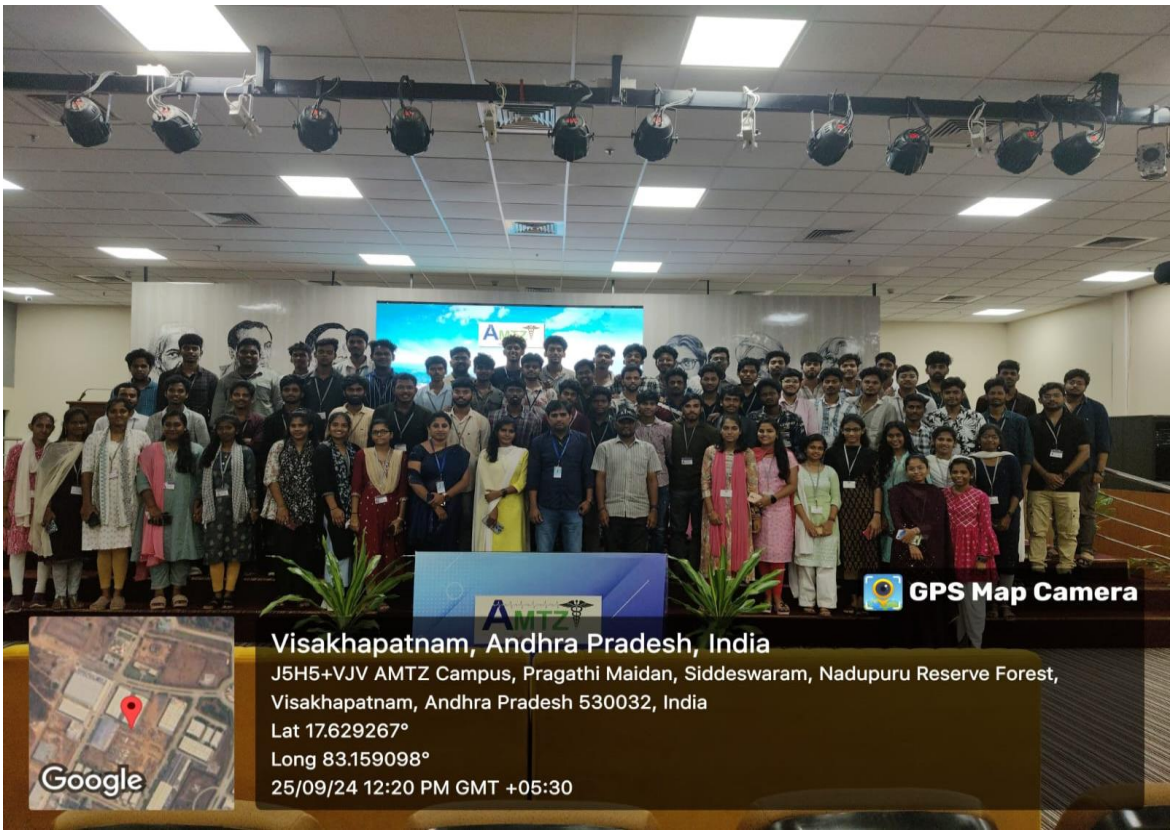
Conclusion

The final day encapsulated the essence of the boot camp—a perfect blend of theory, practical application, and collaborative learning. From the online exam to drone testing, and the heartfelt reflections during the valedictory session, Day 5 highlighted the participants' growth and the program's impact.

The Unmanned Aerial Systems Boot Camp successfully laid a strong foundation for participants to explore advanced applications in drone technology, fostering skills that are essential for future innovations in the field.

Report on Industrial Visit to AMTZ on 25.09.2024

On 25.09.2024, Department of ECE organized an industrial visit to the Andhra Pradesh MedTech Zone (AMTZ) located in Visakhapatnam. The visit aimed to provide participants with insights into the state-of-the-art facilities and infrastructure at AMTZ, as well as to enhance their understanding of the medical technology sector in India.



Students and staff at AMTZ

During the industrial visit, participants were guided through various sections of AMTZ, including:

Research and Development Labs: Participants were introduced to the R&D labs equipped with advanced technology and instrumentation for the development of medical devices. They witnessed ongoing research activities and demonstrations of prototype devices under development.

Testing and Validation Facilities: The visit included a tour of the testing and validation laboratories where medical devices undergo rigorous quality testing and certification processes. Participants gained insights into the standards and protocols followed for ensuring the safety and efficacy of medical devices.

Trainer explaining to the students at AMTZ

Manufacturing Units: Participants visited the manufacturing units within AMTZ, where they observed the production processes for medical devices such as diagnostic equipment, surgical instruments, implants, etc. They learned about the manufacturing techniques, quality control measures, and regulatory compliance requirements.

Incubation Center: The visit also included a visit to the incubation center at AMTZ, which supports startups and entrepreneurs in the medical technology sector. Participants interacted with innovators and entrepreneurs showcasing their innovative ideas and prototypes.

Trainer explaining about 3D Printing to the students

The industrial visit to AMTZ provided participants with several learning outcomes, including: Understanding the importance of indigenous production of medical devices for healthcare self-sufficiency.

HOD,ECE

REPORT ON WORKSHOP

"5G Communications Technology"

Department: Electronics and Communication Engineering (ECE)

Venue: Room No. 611, CSE Department

Dates: 15-11-2024 and 16-11-2024

Resource Person: Mr. Lingeshwaran, Professor, DADB

Participants: IV/IV ECE Students

Total Attendance: 52 Students

Introduction

The Department of Electronics and Communication Engineering organized a two-day workshop on "5G Communications Technology" to provide students with exposure to next-generation wireless communication systems. The workshop aimed to enhance students' understanding of modern communication technologies, applications, and future research opportunities.

Day-1 Session (15-11-2024)

The workshop began with an introductory session on the fundamentals of 5G communication systems, including:

Evolution of wireless communication

Key features of 5G networks

Spectrum usage and bandwidth optimization

Applications of 5G technology

The resource person explained the concepts using presentations and interactive discussions. Students actively participated and clarified their doubts during the session.

Day-2 Session (16-11-2024)

On the second day, the session focused on:

5G architecture and network design

Massive MIMO and IoT integration

Real-world applications of 5G

Career opportunities in communication technology

The session included practical demonstrations, whiteboard explanations, and student interaction, making the workshop highly engaging and informative.

Outcome of the Workshop

Students gained:

Understanding of 5G communication technology

Awareness of industry trends and applications

Knowledge about future communication systems

Motivation to explore research and career opportunities

The workshop was successfully completed with active participation from 52 students.

Conclusion

The workshop on “5G Communications Technology” provided valuable academic and practical exposure to students. The session delivered by Mr. Lingeshwaran (Professor, DADB) helped students understand emerging communication technologies and their applications in real-world scenarios.

The Department of ECE expresses sincere gratitude to the resource person for conducting the workshop successfully.